Quiz EL203
BJTs and FETs

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■ **Note from the author**
I try to keep my materials as brief as possible, usually with no more than 25 exercises; however, here I ended up with 40 problems. The extra size seems justified, though, because mastering the physics and operation of the two main transistor types is one of the main goals of an introductory electronics course. Use the problem distribution table to guide yourself.

PROBLEM DISTRIBUTION

Problems	Subject
1 – 7	Basic BJT problems
8 – 10	BJT emitter-bias configurations
11 – 14	BJT voltage-divider bias configurations
15 – 17	BJT collector-feedback bias configurations
18 - 20	BJT common-base bias configurations
21 - 23	Biasing with *pnp* BJTs
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30	FET fixed-bias configuration
31 – 34	FET self-bias configurations
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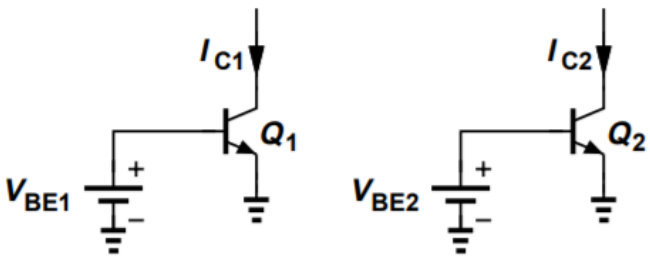
37 - 38	FET common-gate bias configurations
39 - 40	Combination networks

PROBLEMS

Problem 1 (Razavi, 2008, w/ permission)

In the circuit illustrated below, it is observed that the collector currents of Q_1 and Q_2 are equal if the difference of base-emitter voltages is such that $V_{BE1} - V_{BE2} = 20$ mV. Determine the ratio of transistor cross-section areas if the other device parameters are identical.

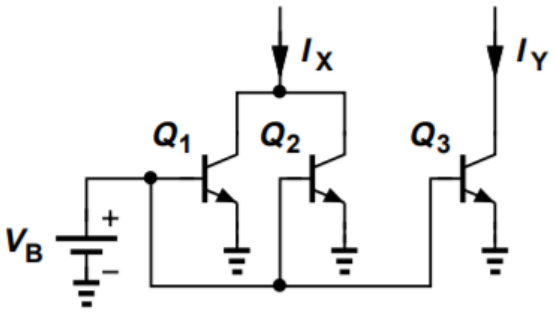


Problem 2 (Razavi, 2008, w/ permission)

For transistors Q_1 and Q_2 in the circuit illustrated below, saturation current parameters $I_{S1} = I_{S2} = 3\times10^{-16}$ A.

Problem 2.1: Calculate base voltage V_B such that $I_X = 1$ mA.

Problem 2.2: With the value of V_B obtained in Problem 2.1, choose a saturation current parameter I_{S3} such that $I_Y = 2.5$ mA.

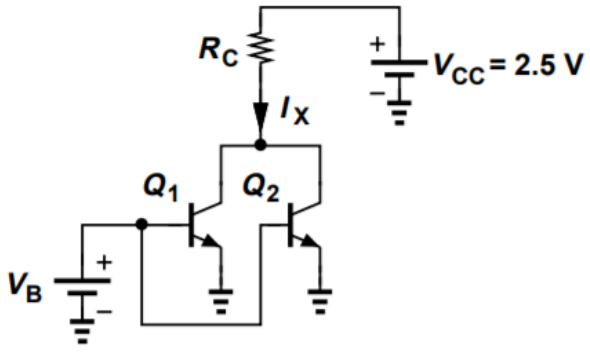


Problem 3 (Razavi, 2008, w/ permission)

Consider the circuit illustrated below.

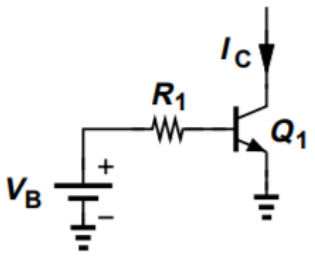
Problem 3.1: If $I_{S1} = 2I_{S2} = 5\times10^{-16}$ A, i.e. the saturation current parameter of Q_1 is twice that of Q_2, find a base voltage V_B such that $I_X = 1.2$ mA.

Problem 3.2: What value of R_C places the transistors at the edge of the active mode?



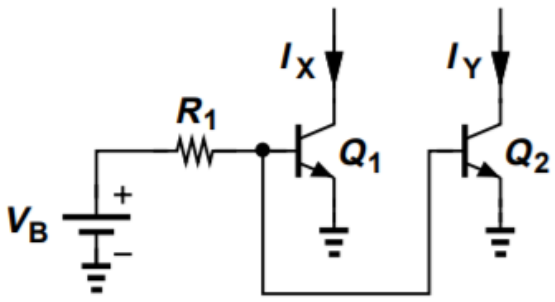
Problem 4 (Razavi, 2008, w/ permission)

Consider the circuit illustrated below, assuming that Q_1 has current gain $\beta = 100$ and saturation current parameter $I_S = 7\times10^{-16}$ A. If $R_1 = 10$ kΩ, determine base voltage V_B such that $I_C = 1$ mA.



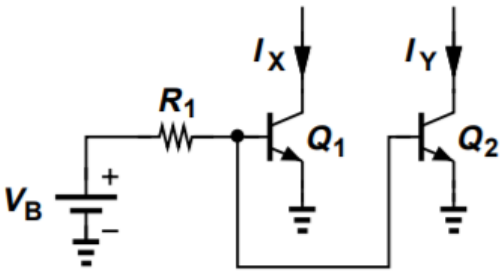
Problem 5 (Razavi, 2008, w/ permission)

In the circuit depicted below, saturation current parameters $I_{S1} = 2I_{S2} = 4\times10^{-16}$ A. If $\beta_1 = \beta_2 = 100$ and $R_1 = 5$ kΩ, compute V_B such that $I_X = 1$ mA.



Problem 6 (Razavi, 2008, w/ permission)

In the circuit illustrated below, $I_{S1} = 3\times10^{-16}$ A, $I_{S2} = 5\times10^{-16}$ A, $\beta_1 = \beta_2 = 100$, $R_1 = 5$ kΩ, and $V_B = 800$ mV. Calculate I_X and I_Y.



Problem 7 (Neamen, 2000, w/ permission)

Problem 7.1: An *npn* bipolar transistor is biased in the forward-active mode. The base current is $I_B = 9.60$ μA and the emitter current is $I_E = 0.780$ mA. Determine the current gain parameter β, the common-base current gain α, and the collector current I_C.

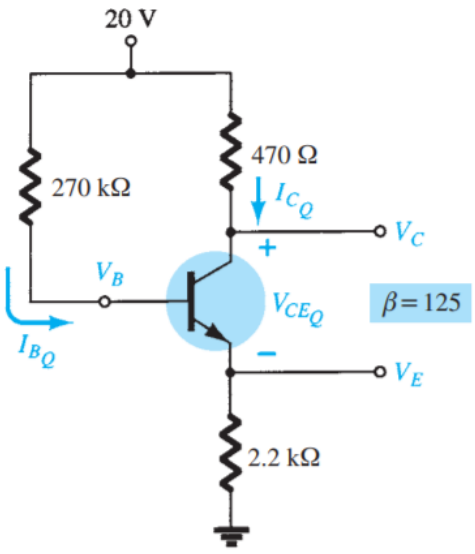
Problem 7.2: The emitter current in a *pnp* bipolar transistor biased in the forward-active mode is $I_E = 2.15$ mA. The common-base current gain of the transistor is $\alpha = 0.990$. Determine β, I_B, and I_C.

Problem 8 (Boylestad and Nashelsky, 2013, w/ permission)

Given the emitter-bias configuration circuit illustrated below, determine:

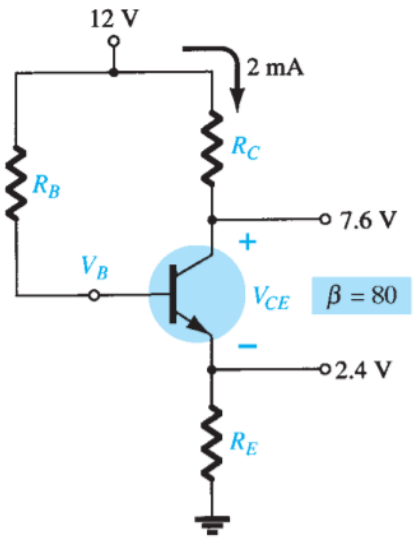
1. Base current I_B.
2. Collector current I_C.
3. Collector-emitter voltage V_{CE}.
4. Collector voltage V_C.

5. Base voltage V_B.
6. Emitter voltage V_E.



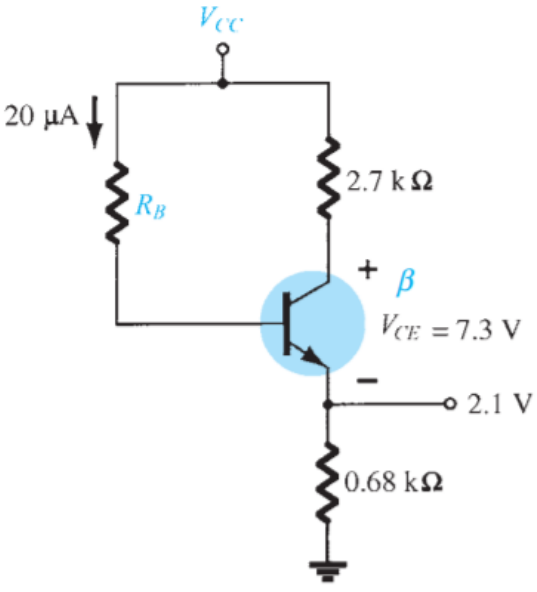
Problem 9 (Boylestad and Nashelsky, 2013, w/ permission)

Given the emitter-bias configuration circuit illustrated below, determine:
1. Collector resistance R_C.
2. Emitter resistance R_E.
3. Base resistance R_B.
4. Collector-emitter voltage V_{CE}.
5. Base voltage V_B.



Problem 10 (Boylestad and Nashelsky, 2013, w/ permission)

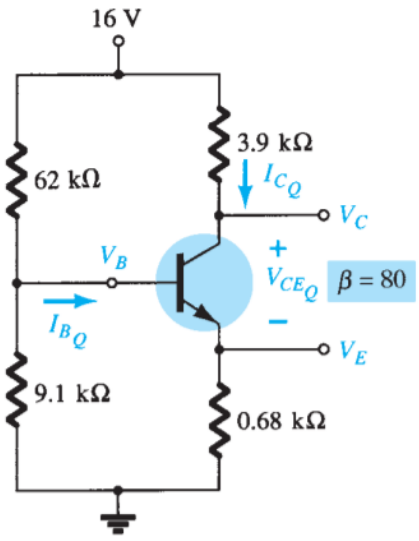
Given the emitter-bias configuration circuit illustrated below, determine:
1. Current gain parameter β.
2. Supply voltage V_{CC}.
3. Base resistance R_B.



Problem 11 (Boylestad and Nashelsky, 2013, w/ permission)

For the voltage-divider bias configuration illustrated below, determine:

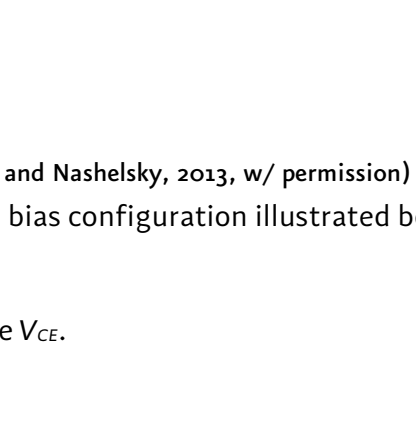
1. Base current I_B.
2. Collector current I_C.
3. Collector-emitter voltage V_{CE}.
4. Collector voltage V_C.
5. Emitter voltage V_E.
6. Base voltage V_B.



Problem 12 (Boylestad and Nashelsky, 2013, w/ permission)

For the voltage-divider bias configuration illustrated below, determine:

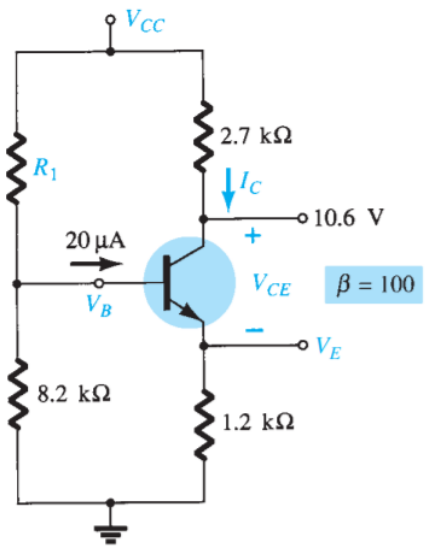
1. Collector current I_C.
2. Emitter voltage V_E.
3. Base voltage V_B.
4. Resistance R_1.



Problem 13 (Boylestad and Nashelsky, 2013, w/ permission)

For the voltage-divider bias configuration illustrated below, determine:

1. Collector current I_C.
2. Emitter voltage V_E.
3. Supply voltage V_{CC}.
4. Collector-emitter voltage V_{CE}.
5. Base voltage V_B.
6. Resistance R_1.

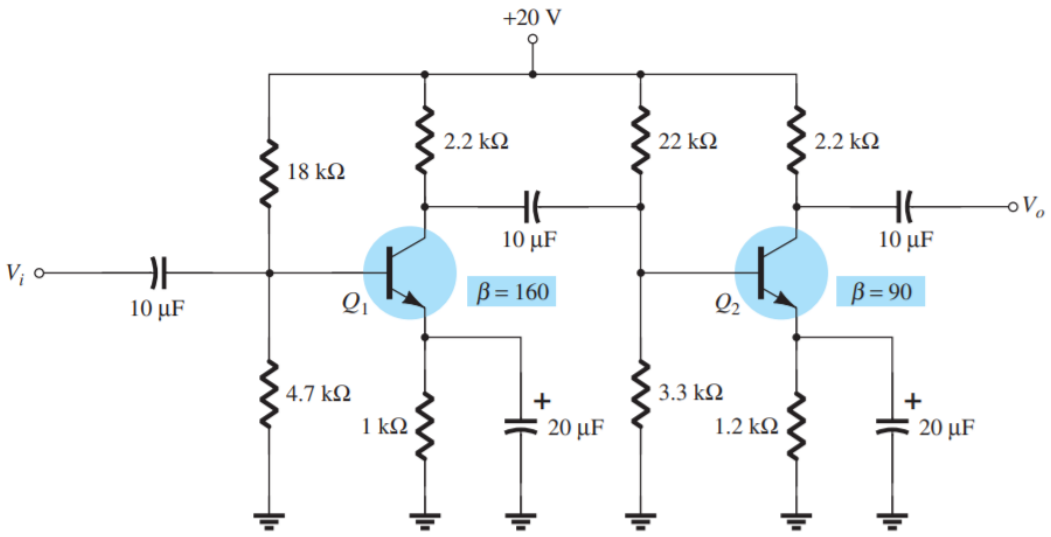


Problem 14 (Boylestad and Nashelsky, 2013, w/ permission)

For the *R-C* coupled amplifier illustrated below, determine:

1. The voltages V_B, V_C, and V_E for each transistor.

2. The currents I_B, I_C, and I_E for each transistor.



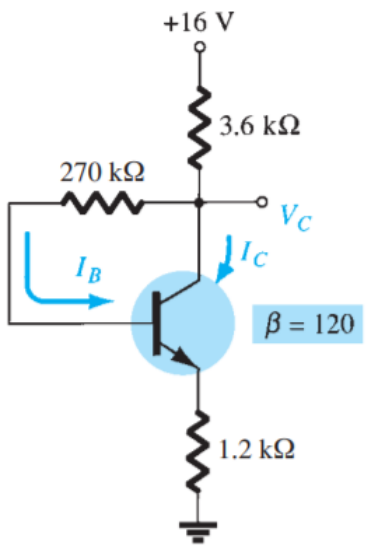
Problem 15 (Boylestad and Nashelsky, 2013, w/ permission)

For the collector-feedback configuration illustrated below, determine:

1. Base current I_B.

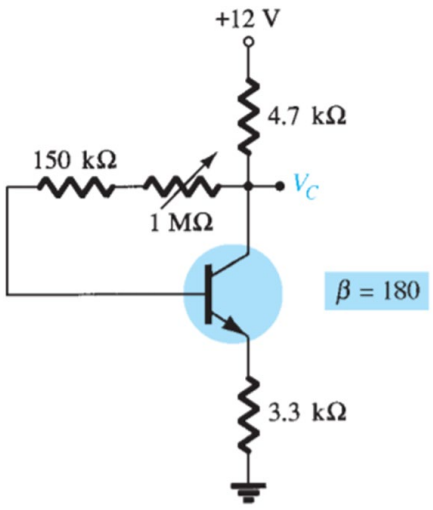
2. Collector current I_C.

3. Collector voltage V_C.



Problem 16 (Boylestad and Nashelsky, 2013, w/ permission)

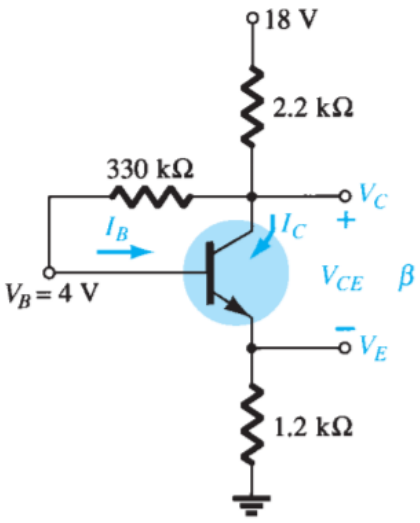
Determine the range of possible values for the collector-to-ground voltage V_C for the network illustrated below, considering the potentiometer in the collector-feedback loop varies from zero to 1 MΩ.



Problem 17 (Boylestad and Nashelsky, 2013, w/ permission)

Given $V_B = 4$ V for the collector-feedback configuration illustrated below, determine:

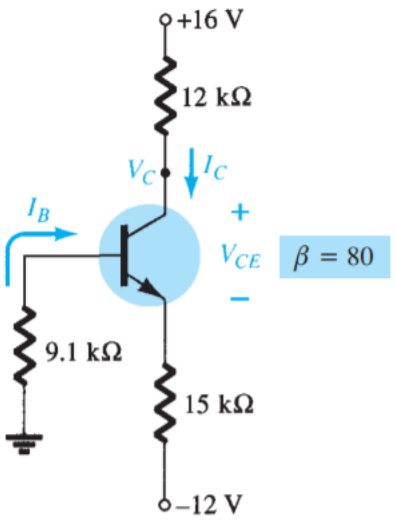
1. Emitter voltage V_E.
2. Collector current I_C.
3. Collector voltage V_C.
4. Collector-emitter voltage V_{CE}.
5. Base current I_B.
6. Current gain parameter β.



Problem 18 (Boylestad and Nashelsky, 2013, w/ permission)

For the common-base configuration illustrated below, determine:

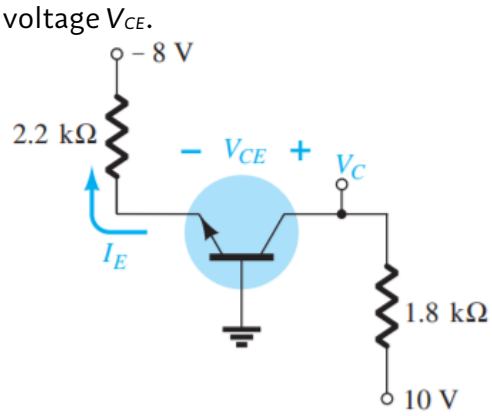
1. Base current I_B.
2. Collector current I_C.
3. Collector-emitter voltage V_{CE}.
4. Collector voltage V_C.



Problem 19 (Boylestad and Nashelsky, 2013, w/ permission)

For the common-base configuration illustrated below, determine:

1. Emitter current I_E.
2. Collector voltage V_C.
3. Collector-emitter voltage V_{CE}.



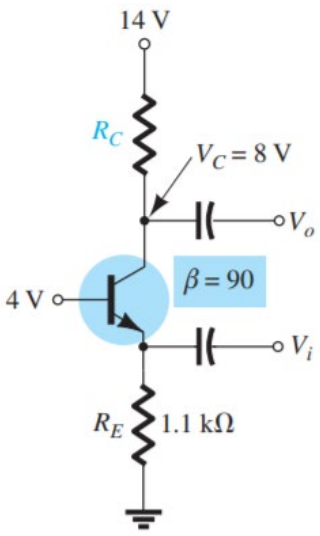
Problem 20 (Boylestad and Nashelsky, 2013, w/ permission)

For the common-base network illustrated below,

1. Using the information provided, determine the value of R_C.

2. Find the currents I_B and I_E.

3. Determine the voltages V_{BC} and V_{CE}.



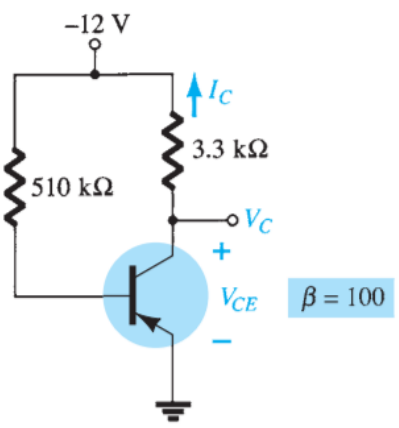
Problem 21 (Boylestad and Nashelsky, 2013, w/ permission)

An emitter-bias configuration with a *pnp* bipolar transistor is illustrated to the side. Determine:

1. Collector voltage V_C.

2. Collector-emitter voltage V_{CE}.

3. Collector current I_C.

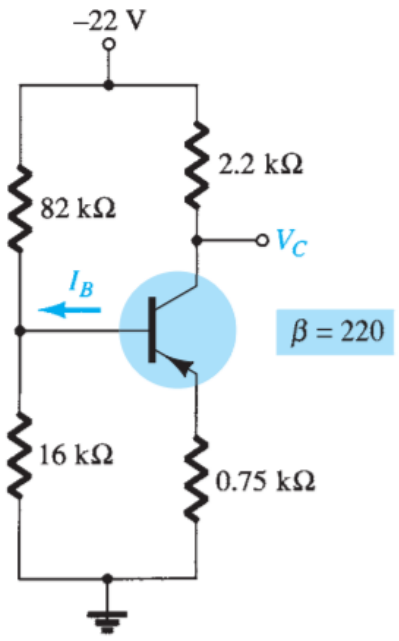


Problem 22 (Boylestad and Nashelsky, 2013, w/ permission)

A voltage-divider bias configuration with a *pnp* bipolar transistor is illustrated below. Determine:

1. Collector voltage V_C.

2. Base current I_B.

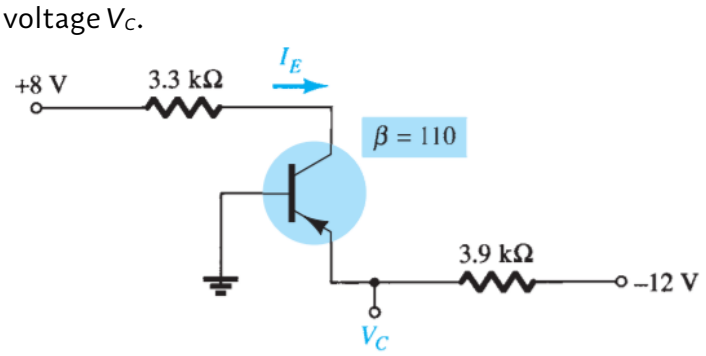


Problem 23 (Boylestad and Nashelsky, 2013, w/ permission)

A common-base configuration with a *pnp* bipolar transistor is illustrated below. Determine:

1. Emitter current I_E.

2. Collector voltage V_C.



Problem 24 (Neamen, 2000, w/ permission)

Consider an *n*-channel enhancement-mode MOSFET with threshold voltage V_{TN} = 1.5 V and MOSFET conduction parameter K_n = 0.25 mA/V^2. Determine the drain current I_D for the following voltage combinations:
Problem 24.1: Gate-source voltage V_{GS} = 5 V, drain-source voltage V_{DS} = 6 V.
Problem 24.2: Gate-source voltage V_{GS} = 5 V, drain-source voltage V_{DS} = 2.5 V.

Problem 25 (Neamen, 2000, w/ permission)

The parameters of an *n*-channel enhancement-mode MOSFET are threshold voltage V_{TN} = 0.8 V, process transconductance parameter k_n' = 80 μA/V^2, and aspect ratio W/L = 5. Assume the transistor is biased in the saturation region and drain current I_D = 0.5 mA. Determine the drain-source voltage at saturation, $V_{DS}(sat)$, and the required gate-source voltage, V_{GS}.

Problem 26 (Neamen, 2000, w/ permission)

An *n*-channel enhancement-mode MOSFET has threshold voltage V_{TN} = 0.8 V, channel width W = 64 μm, channel length L = 4 μm, oxide thickness t_{ox} = 450 Å, and electron mobility μ_n = 650 cm^2/V-s. Use 3.9 as the relative permittivity of silicon.
Problem 26.1: Calculate the MOSFET conduction parameter, K_n.
Problem 26.2: Determine the drain current I_D when $V_{GS} = V_{DS}$ = 3 V (i.e., both gate-source and drain-source voltages equal 3 V).

Problem 27 (Neamen, 2000, w/ permission)

A particular NMOS device has threshold voltage V_{TN} = 1 V, channel length L = 2.5 μm, oxide layer thickness t_{ox} = 400 Å, and electron mobility μ_n = 600 cm^2/V-s. A drain current of I_D = 1.2 mA is required when the device is biased in the saturation region at V_{GS} = 5 V. Determine the necessary channel width of the device.

Problem 28 (Neamen, 2000, w/ permission)

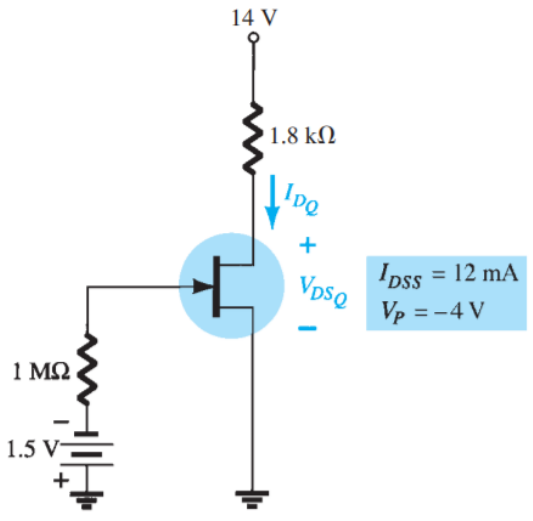
Consider a *p*-channel depletion-mode MOSFET with FET conduction parameter K_p = 0.5 mA/V^2 and threshold voltage V_{TP} = +2 V. If source-gate voltage V_{SG} = 0, determine the drain current for source-drain voltages V_{SD} = 1 V, V_{SD} = 2 V, and V_{SD} = 3 V.

Problem 29 (Neamen, 2000, w/ permission)

Enhancement-mode NMOS and PMOS devices both have channel length L = 4 μm and oxide thickness t_{ox} = 500 Å. For the NMOS transistor, threshold voltage V_{TN} = +0.6 V, electron mobility μ_n = 675 cm^2/V-s, and the channel width is W_n. For the PMOS transistor, threshold voltage V_{TP} = −0.6 V, electron mobility μ_p = 375 cm^2/s, and the channel width is W_p. Design the widths of the two transistors such that they are electrically equivalent and the drain current in the PMOS transistor is I_D = 0.8 mA when it is biased in the saturation region with V_{SG} = 5 V. What are the values of the NMOS conduction parameter K_n, PMOS conduction parameter K_p, channel width W_n, and channel width W_p? Use 3.9 as the relative permittivity of silicon.

Problem 30 (Boylestad and Nashelsky, 2013, w/ permission)

For the fixed-bias configuration illustrated below:
1. Sketch the transfer curve for the device.
2. Superimpose the network equation on the same graph.
3. Determine the quiescent drain current I_{D_Q} and the quiescent gate-source voltage V_{DS_Q}.
4. Using Shockley's equation, solve for I_{D_Q} and then find V_{DS_Q}. How does this mathematical approach compare to the graphical method?



Problem 31 (Boylestad and Nashelsky, 2013, w/ permission)

For the self-bias configuration illustrated below:

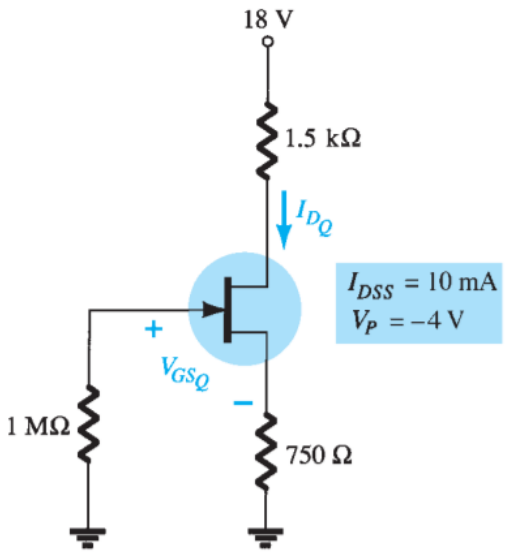
1. Sketch the transfer curve for the device.

2. Superimpose the network equation on the same graph.

3. Determine the quiescent drain current I_{D_Q} and the quiescent gate-source voltage V_{GS_Q}.

4. Using the *Q*-point data, determine the drain-source voltage V_{DS}, the drain voltage V_D, the gate voltage V_G, and the source voltage V_S.

5. Determine the *Q*-point drain current and gate-source voltage directly, using a mathematical approach. How do the results compare with the graphical approach?

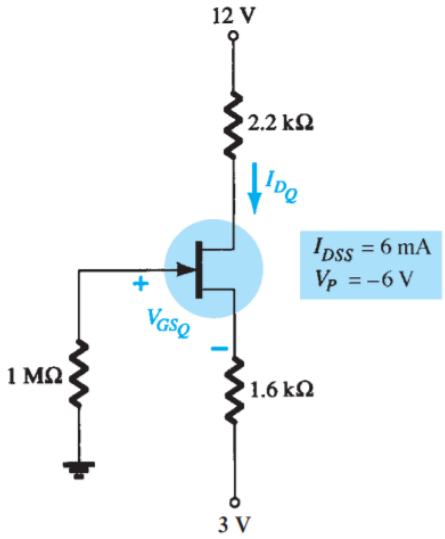


Problem 32 (Boylestad and Nashelsky, 2013, w/ permission)

For the self-bias configuration illustrated below:

1. Determine the quiescent drain current I_{D_Q} and the quiescent gate-source voltage V_{GS_Q}.

2. Using the *Q*-point data, determine the drain-source voltage V_{DS}, the drain voltage V_D, the gate voltage V_G, and the source voltage V_S.



Problem 33 (Boylestad and Nashelsky, 2013, w/ permission)

Given the measurement V_S = 1.7 V for the self-bias network illustrated to the side, determine:

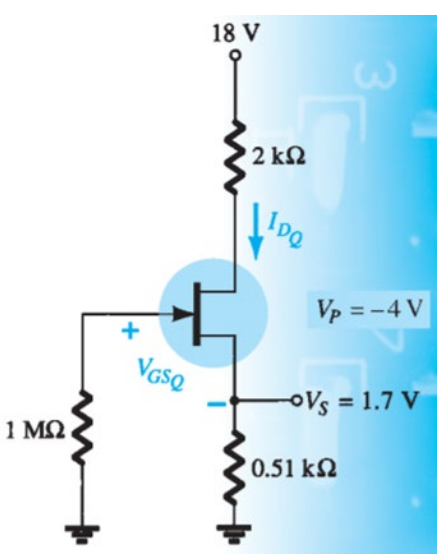
1. Quiescent drain current, I_{D_Q}.

2. Quiescent gate-source voltage, V_{GS_Q}.

3. Maximum drain-source current, I_{DSS}.

4. Drain voltage, V_D.

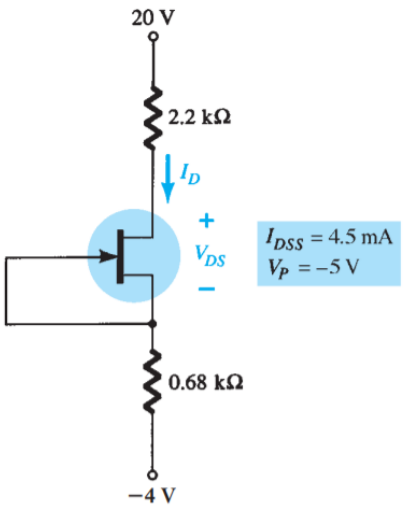
5. Drain-source voltage, V_{DS}.



Problem 34 (Boylestad and Nashelsky, 2013, w/ permission)

In the special self-bias configuration illustrated below, determine:

1. Drain current I_D.
2. Drain-source voltage V_{DS}.
3. Drain voltage V_D.
4. Source voltage V_S.

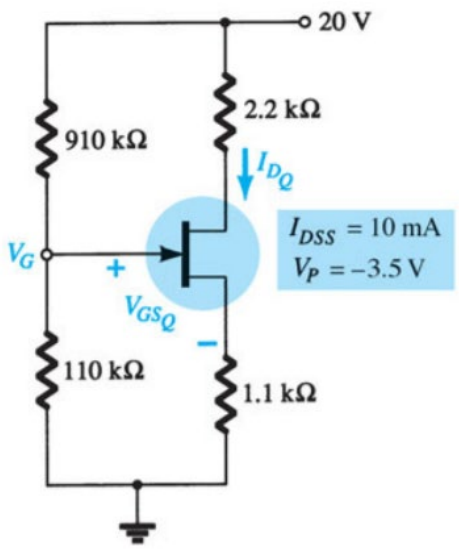


Problem 35 (Boylestad and Nashelsky, 2013, w/ permission)

Problem 35.1: For the voltage-divider biasing network illustrated below, determine:

1. Gate-to-ground voltage, V_G.
2. Quiescent drain current, I_{D_Q}, and the quiescent gate-source voltage, V_{GS_Q}.
3. Drain voltage, V_D, and source voltage, V_S.
4. Quiescent drain-source voltage, V_{DS_Q}.

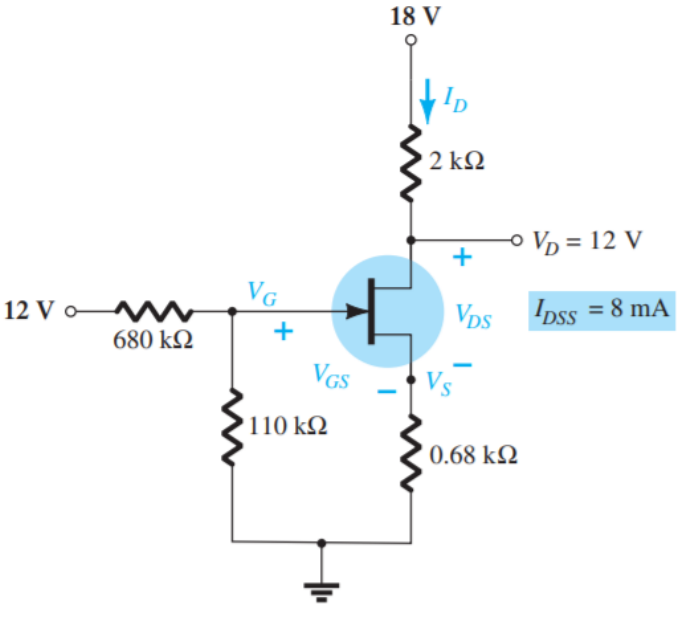
Problem 35.2: Replace the 1.1-kΩ source resistance $R_S' = 0.51$ kΩ (about 50% of the value used previously). What is the effect of a smaller R_S on the quiescent values I_{D_Q} and V_{GS_Q}?



Problem 36 (Boylestad and Nashelsky, 2013, w/ permission)

For the voltage-divider bias network illustrated below, $V_D = 10$ V. Determine:

1. Drain current, I_D.
2. Source voltage, V_S, and drain-source voltage, V_{DS}.
3. Gate voltage, V_G, and gate-source voltage, V_{GS}.
4. The FET's pinch-off voltage, V_P.

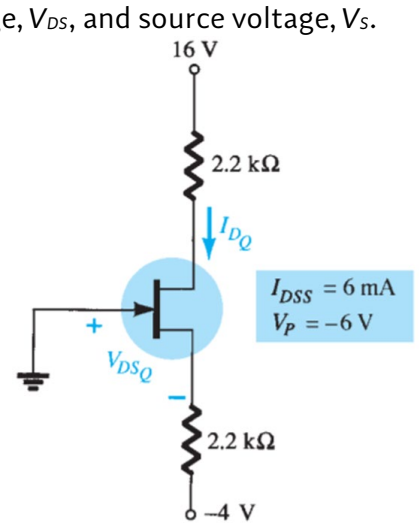


Problem 37 (Boylestad and Nashelsky, 2013, w/ permission)

For the common-gate configuration illustrated below, determine:

1. Quiescent drain current, I_{D_Q}, and quiescent gate-source voltage, V_{GS_Q}.

2. Drain-source voltage, V_{DS}, and source voltage, V_S.



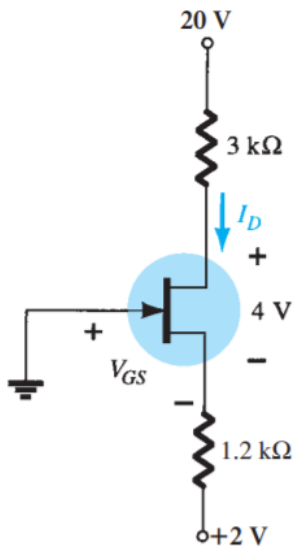
Problem 38 (Boylestad and Nashelsky, 2013, w/ permission)

Given V_{DS} = 4 V for the common-gate configuration illustrated below, determine:

1. Drain current, I_D.

2. Drain voltage, V_D, and source voltage, V_S.

3. Gate-source voltage, V_{GS}.



Problem 39 (Boylestad and Nashelsky, 2013, w/ permission)

For the combination network illustrated below, determine:

1. Gate voltage, V_G.

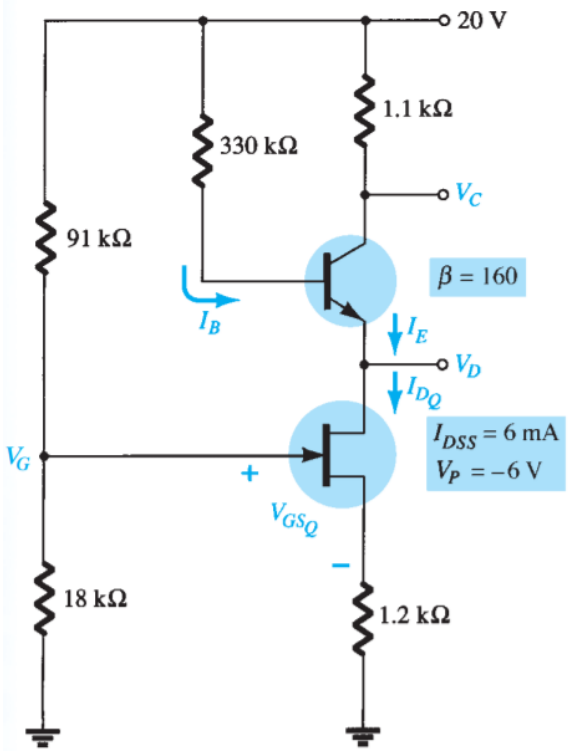
2. Quiescent gate-source voltage, V_{GS_Q}, and drain current, I_{D_Q}.

3. Emitter current, I_E.

4. Base current, I_B.

5. Drain voltage, V_D.

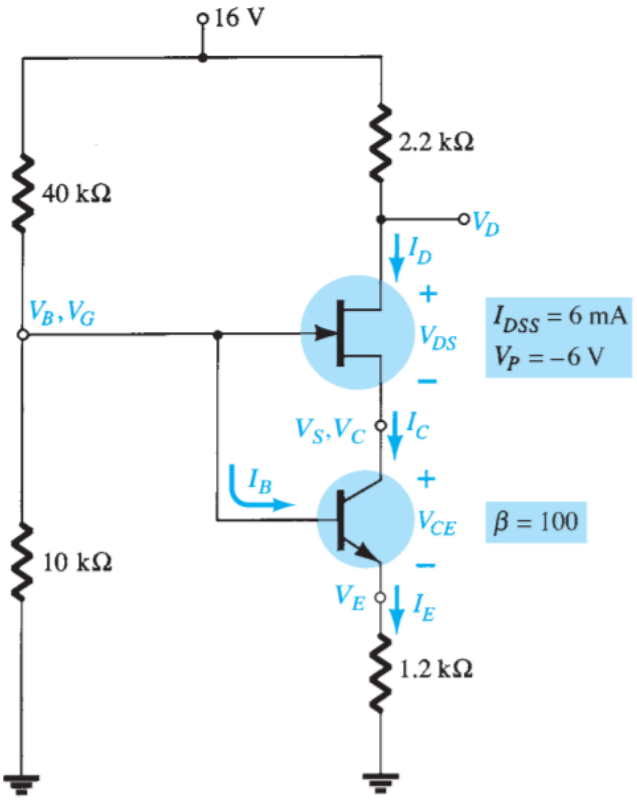
6. Collector voltage, V_C.



Problem 40 (Boylestad and Nashelsky, 2013, w/ permission)

For the combination network illustrated below, determine:

1. Base voltage, V_B, and gate voltage, V_G.
2. Emitter voltage, V_E.
3. Emitter current, I_E, collector current, I_C, and drain current, I_D.
4. Base current, I_B.
5. Collector voltage, V_C, source voltage, V_S, and drain voltage, V_D.
6. Collector-emitter voltage, V_{CE}.
7. Drain-source voltage, V_{DS}.



SOLUTIONS

P.1 ➡ *Solution*

The collector current can be estimated as

$$I_C = \frac{A_E q D_n n_i^2}{N_B W_B}\left(e^{V_{BE}/V_T} - 1\right)$$

Here, A_E is the emitter cross-section area, q is elementary charge, D_n is the electron diffusion coefficient, n_i is intrinsic carrier concentration, N_B is the dopant concentration in the base region, W_B is the width of the base region, V_{BE} is base-emitter voltage, and V_T is thermal voltage. With $exp(V_{BE}/V_T) \gg 1$, we can propose the approximation

$$I_C \approx \frac{A_E q D_n n_i^2}{N_B W_B} e^{V_{BE}/V_T}$$

Now, noting that $I_{C_1} = I_{C_2}$ when $V_{BE1} - V_{BE2}$, we may write

$$I_{C_1} = I_{C_2} \rightarrow \frac{A_{E,1} q D_n n_i^2}{N_B W_B} e^{V_{BE,1}/V_T} = \frac{A_{E,2} q D_n n_i^2}{N_B W_B} e^{V_{BE,2}/V_T}$$

$$\therefore \frac{e^{V_{BE,1}/V_T}}{e^{V_{BE,2}/V_T}} = \frac{\dfrac{A_{E,2} \cancel{q D_n n_i^2}}{\cancel{N_B W_B}}}{\dfrac{A_{E,1} \cancel{q D_n n_i^2}}{\cancel{N_B W_B}}} = \frac{A_{E,2}}{A_{E,1}}$$

$$\therefore e^{\left(V_{BE,1} - V_{BE,2}\right)/V_T} = \frac{A_{E,2}}{A_{E,1}}$$

$$\therefore \frac{A_{E,2}}{A_{E,1}} = e^{20/26} = \boxed{2.16}$$

Thus, for the two devices to have equal collector currents when $V_{BE1} - V_{BE2} = 20$ mV, the emitter cross-section of one must be about 2.16 times larger than that of the other.

P.2 ➡ Solution

Problem 2.1: If devices Q_1 and Q_2 have the same saturation current parameters, it is reasonable to assume that they are identical and therefore share the incoming collector current I_X equally,

$$I_{Q_1} = I_{Q_2} = 0.5\,\text{mA}$$

Writing the current-voltage relationship for either device, we solve for V_B and obtain

$$I_{Q_1} = I_{S_1} e^{V_B/V_T} \rightarrow V_B = V_T \ln\left(\frac{I_{Q_1}}{I_{S_1}}\right)$$

$$\therefore V_B = 26 \times \ln\left(\frac{0.5\times10^{-3}}{3\times10^{-16}}\right) = \boxed{732\,\text{mV}}$$

Problem 2.2: Device 3 conducts a collector current I_Y = 2.5 mA and is subjected to a voltage V_B = 732 mV determined just now. Accordingly, we may prescribe a saturation current parameter I_{S3} such that

$$I_{Q_3} = I_Y = I_{S_3} e^{V_B/V_T} \rightarrow I_{S_3} = \frac{I_Y}{e^{V_B/V_T}}$$

$$\therefore I_{S_3} = \frac{2.5\times10^{-3}}{e^{732/26}} = \boxed{1.48\times10^{-15}\ \text{A}}$$

or 1.48 fA.

P.3 ➡ Solution

Problem 3.1: Per Kirchhoff's current law, I_X separates into two components I_1 and I_2 fed into the collector junction of transistors Q_1 and Q_2, respectively. Appealing to the current-voltage relationship and solving for V_B, we find that

$$I_X = I_1 + I_2 \rightarrow I_X = I_{S1} e^{V_B/V_T} + I_{S2} e^{V_B/V_T}$$

$$\therefore I_X = \left(\underbrace{I_{S1}}_{=2I_{S2}} + I_{S2}\right) e^{V_B/V_T}$$

$$\therefore I_X = 3I_{S2} e^{V_B/V_T}$$

$$\therefore V_B = V_T \ln\left(\frac{I_X}{3I_{S2}}\right) = 26\times\ln\left[\frac{1.2\times10^{-3}}{3\times\left(\frac{5}{2}\times10^{-16}\right)}\right] = \boxed{731\,\text{mV}}$$

Problem 3.2: At the edge of the active mode, the collector junction voltage just equals the base voltage, that is, $V_C \approx V_B$. Applying Kirchhoff's voltage law to the collector-base junction of either transistor and solving for resistance R_C, we get

$$V_{CC} - R_C I_X = \underbrace{V_C}_{\rightarrow V_B} \rightarrow R_C = \frac{V_{CC} - V_B}{I_X}$$

$$\therefore R_C = \frac{2.5 - 0.731}{1.2\times10^{-3}} = 1470\,\Omega = \boxed{1.47\,\text{k}\Omega}$$

P.4 ➡ Solution

Applying Kirchhoff's voltage law to the base-emitter junction of Q_1, we obtain

$$V_B - R_1 I_B = V_{BE,\,Q_1}$$

Solving for V_B,

$$V_B = V_{BE,\,Q_1} + 10{,}000 I_B \quad \text{(I)}$$

If collector current I_C is set to 1 mA and the current gain parameter of Q_1 is β = 100, it follows that $I_B = I_C/\beta$ = 0.01 mA. Appealing to the current-voltage relationship, the base-emitter voltage V_{BE,Q_1} is calculated as

$$I_C = I_S e^{V_{BE,Q_1}/V_T} \rightarrow V_{BE,Q_1} = V_T \ln\left(\frac{I_C}{I_S}\right)$$

$$\therefore V_{BE,Q_1} = 26\times\ln\left(\frac{1.0\times10^{-3}}{7.0\times10^{-16}}\right) = 728\text{ mV}$$

Substituting in (I), we get

$$V_B = 0.728 + 10{,}000\times\left(0.01\times10^{-3}\right) = \boxed{0.828\text{ V}}$$

Thus, Q_1 will conduct a collector current of 1 mA if base voltage V_B is set to ~0.83 V.

P.5 ➡ *Solution*

Writing current-voltage relationships for Q_1 and Q_2, we have, respectively,

$$I_X = I_{S1}e^{V_{BE,1}/V_T}\ \ ;\ \ I_Y = I_{S2}e^{V_{BE,2}/V_T}$$

Dividing one equation by the other and noting that $V_{BE1} = V_{BE2} = V_{BE}$, we get

$$\frac{I_X}{I_Y} = \frac{I_{S1}\cancel{e^{-V_{BE}/V_T}}}{I_{S2}\cancel{e^{-V_{BE}/V_T}}} = \frac{2I_{S2}}{I_{S2}} = 2$$

Noting that $I_X = \beta_1 I_{B1}$, $I_Y = \beta_2 I_{B2}$, and $\beta_1 = \beta_2 = \beta$, the ratio above can be restated as

$$\frac{I_X}{I_Y} = 2 \rightarrow \frac{\cancel{\beta} I_{B1}}{\cancel{\beta} I_{B2}} = 2$$

$$I_{B1} = 2I_{B2}$$

If $I_X = 1$ mA, it follows that

$$I_{B1} = \frac{I_X}{\beta} = \frac{1.0\times10^{-3}}{100} = 10^{-5}\text{ A} = 10\,\mu\text{A}$$

and

$$I_{B2} = \frac{I_{B1}}{\beta} = 5\,\mu\text{A}$$

Applying KVL in the base branch of the circuit, we obtain

$$V_B - \left(I_{B1} + I_{B2}\right)R_1 = V_{BE} \rightarrow V_B = V_{BE} + \left(I_{B1} + I_{B2}\right)R_1$$

The only missing quantity in the equation above is V_{BE}, which can be determined as

$$I_X = I_{S1}e^{V_{BE}/V_T} \rightarrow V_{BE} = V_T\ln\left(\frac{I_X}{I_{S1}}\right)$$

$$\therefore V_{BE} = 26\times\ln\left(\frac{1.0\times10^{-3}}{4.0\times10^{-16}}\right) = 742\,\text{mV}$$

so that

$$V_B = V_{BE} + \left(I_{B1} + I_{B2}\right)R_1 = 0.742 + \left[\left(10\times10^{-6}\right) + \left(5\times10^{-6}\right)\right]\times\left(5\times10^{3}\right) = \boxed{0.817\text{ V}}$$

The base must be fed a voltage of ~0.82 V.

P.6 ➡ *Solution*

First, note that base-emitter voltage $V_{BE1} = V_{BE2} = V_{BE}$. With $I_{B1} = I_X/\beta$, $I_{B2} = I_Y/\beta$, and $V_{BE} = V_T\ln(I_X/I_{S1})$, we apply KVL to the base region of the transistors to obtain

$$V_B = \left(I_{B1} + I_{B2}\right)R_1 + V_{BE} \rightarrow V_B = \frac{R_1}{\beta}\left(I_X + I_Y\right) + V_T\ln\left(\frac{I_X}{I_{S1}}\right)$$

$$\therefore 0.8 = \frac{5000}{100}\times\left(I_X + I_Y\right) + 0.026\times\ln\left(\frac{I_X}{3\times10^{-16}}\right)$$

If $I_{S1} = 3\times10^{-16}$ A and $I_{S2} = 5\times10^{-16}$ A, it is easy to see that $I_Y = 5I_X/3$. Substituting above gives

$$0.8 = \frac{5000}{100}\times\left(I_X + \frac{5I_X}{3}\right) + 0.026\times\ln\left(\frac{I_X}{3\times10^{-16}}\right)$$

$$\therefore 0.8 = 50\times\frac{8I_X}{3} + 0.026\times\ln\left(\frac{I_X}{3\times10^{-16}}\right)$$

$$\therefore 0.8 = \frac{400 I_X}{3} + 0.026 \times \ln\left(\frac{I_X}{3\times 10^{-16}}\right)$$

The result above is a transcendental equation in I_X. One way to solve it is via MATLAB's *fsolve* command:

```
function y = current(IX)
y = 0.8 - 400*IX/3 - 0.026*log(IX/3E-16);

>> fun = @current;
x0 = 1E-3;
z = fsolve(fun,x0)
```

This code returns $I_X \approx 5.09\times10^{-4}$ A = 509 μA. Lastly, using $I_Y = 5I_X/3$ yields

$$I_Y = \frac{5I_X}{3} = \frac{5\times 509}{3} = \boxed{848\,\mu\text{A}}$$

P.7 ➡ *Solution*

Problem 7.1: The collector current is determined as

$$I_E = I_C + I_B \rightarrow I_C = I_E - I_B$$

$$\therefore I_C = 0.780 - 0.0096 = \boxed{0.770\,\text{mA}}$$

Next, the current gain parameter β is given by the ratio

$$I_C = \beta I_B \rightarrow \beta = \frac{I_C}{I_B}$$

$$\therefore \beta = \frac{0.770}{0.0096} = \boxed{80.2}$$

Using β, we can determine the common-base current gain α,

$$\alpha = \frac{\beta}{1+\beta} = \frac{80.2}{1+80.2} = \boxed{0.9877}$$

Problem 7.2: The common-base current gain parameter α can be used to determine β,

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.990}{1-0.990} = \boxed{99.0}$$

Next, the collector current I_C is given by the ratio

$$I_C = \alpha I_E = 0.990\times 2.15 = \boxed{2.13\,\text{mA}}$$

Then, the only missing current component is I_B,

$$I_E = I_C + I_B \rightarrow I_B = I_E - I_C$$

$$\therefore I_B = 2.15 - 2.13 = 0.02\ \text{mA} = \boxed{20\,\mu\text{A}}$$

P.8 ➡ *Solution*

Applying Kirchhoff's voltage law to the base-emitter loop, we obtain

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \rightarrow V_{CC} - I_B R_B - V_{BE} - (\beta+1) I_B R_E = 0$$

$$\therefore -I_B\left[R_B + (\beta+1)R_E\right] + V_{CC} - V_{BE} = 0$$

$$\therefore I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_E} = \frac{20 - 0.7}{270 + (125+1)\times 2.2} = 0.0353\,\text{mA} = \boxed{35.3\,\mu\text{A}}$$

Using the current gain parameter, we can establish the collector current

$$I_{C_Q} = \beta I_{B_Q} = 125\times 35.3 = 4410\,\mu\text{A} = \boxed{4.41\,\text{mA}}$$

The collector-emitter voltage can be obtained by applying KVL to, wait for it, the collector-emitter junction:

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0 \rightarrow V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

Using $I_E \approx I_C$,

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \rightarrow V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$\therefore V_{CE} = 20 - 4.41\times(0.470 + 2.2) = \boxed{8.23\,\text{V}}$$

To determine the collector-to-ground voltage, apply KVL to the collector-emitter junction a second time, then note that $V_{CC} - I_C R_C = V_C$,

$$V_{CE} = \underbrace{V_{CC} - I_C R_C}_{=V_C} - I_E R_E \rightarrow V_{CE} = V_C - I_E R_E$$

$$\therefore V_C = V_{CE} + \underbrace{I_E}_{=I_C} R_E = 8.23 + 4.41 \times 2.2 = \boxed{17.93\ \text{V}}$$

To determine the base voltage V_B, apply KVL starting at the supply node V_{CC} and ending at the V_B node,

$$V_B = V_{CC} - I_B R_B = 20 - 0.0353 \times 270 = \boxed{10.47\ \text{V}}$$

To determine the emitter voltage V_E, simply appeal to the definition of V_{CE},

$$V_{CE} = V_C - V_E \rightarrow V_E = V_C - V_{CE}$$

$$\therefore V_E = 17.93 - 8.23 = \boxed{9.7\ \text{V}}$$

P.9 ➡ Solution

To determine R_C, apply KVL to the segment joining the 12-V voltage source to the collector node $V_C = 7.6$ V,

$$12 - \left(2.0 \times 10^{-3}\right) R_C = 7.6 \rightarrow R_C = \frac{12 - 7.6}{2.0 \times 10^{-3}} = \boxed{2.2\,\text{k}\Omega}$$

To determine R_E, note that the potential difference across this resistor is 2.4 V. Also, using $I_C = 2$ mA and $\beta = 80$, we can determine the current flowing through this resistor,

$$I_E = \left(\frac{\beta + 1}{\beta}\right) I_C = \left(\frac{80 + 1}{80}\right) \times 2.0 = 2.03\,\text{mA}$$

so that

$$R_E = \frac{2.4}{2.03 \times 10^{-3}} = \boxed{1.18\,\text{k}\Omega}$$

The current flowing through the base resistance is

$$I_B = I_E - I_C = 2.03 - 2.0 = 0.03\,\text{mA} = 30\,\mu\text{A}$$

and can be used to determine the value of R_B,

$$12 - I_B R_B = V_B \rightarrow 12 - I_B R_B = V_{BE} + V_E$$

$$\therefore 12 - 0.03 R_B = 0.7 + 2.4$$

$$\therefore R_B = \frac{12 - \left(0.7 + 2.4\right)}{0.03} = \boxed{297\,\text{k}\Omega}$$

By inspection, the collector-emitter voltage is

$$V_{CE} = V_C - V_E = 7.6 - 2.4 = \boxed{5.2\ \text{V}}$$

The base-to-ground voltage is

$$V_B = V_{BE} + V_E = 0.7 + 2.4 = \boxed{3.1\,\text{V}}$$

P.10 ➡ Solution

Applying KVL to the emitter junction, we obtain

$$2.1 - 0.68 \times I_E = 0 \rightarrow I_E = \frac{2.1}{0.68} = 3.09\,\text{mA}$$

We also have the base current $I_B = 20$ μA; thus, the current gain parameter easily follows,

$$I_E = \left(1 + \beta\right) I_B \rightarrow \beta = \frac{I_E}{I_B} - 1 = \frac{3.09}{20 \times 10^{-3}} - 1 = \boxed{154}$$

Now, if $V_E = 2.1$ V and $V_{CE} = 7.3$ V, the collector-to-ground voltage is found as

$$V_{CE} = V_C - V_E \rightarrow V_C = V_{CE} + V_E$$

$$\therefore V_C = 7.3 + 2.1 = 9.4\,\text{V}$$

so that, using KVL on the collector branch of the circuit, we can determine supply voltage V_{CC},

$$V_{CC} - I_C \times 2.7 = V_C \rightarrow V_{CC} = V_C + \underbrace{I_C}_{\approx I_E} \times 2.7$$

$$\therefore V_{CC} = 9.4 + I_E \times 2.7 = 9.4 + 3.09 \times 2.7 = \boxed{17.74\,\text{V}}$$

Lastly, we apply KVL to the base branch,

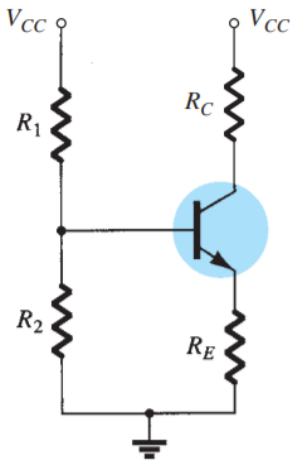
$$V_{CC} - I_B R_B = \underbrace{V_B}_{=0.7+V_E} \rightarrow V_{CC} - I_B R_B = 0.7 + V_E$$

$$\therefore R_B = \frac{V_{CC} - (0.7 + V_E)}{I_B} = \frac{17.74 - (0.7 + 2.1)}{20 \times 10^{-6}} = 7.47 \times 10^5\ \Omega = \boxed{747\,\text{k}\Omega}$$

P.11 ➡ *Solution*

It can be shown that in the present case βR_E is not greater than $10R_2$, which means that the approximate solution is not valid. Instead, we must proceed with the exact approach.

We first establish a Thévenin equivalent resistance given by (see figure to the side for notation)



$$R_{\text{Th}} = R_1 \,||\, R_2 = \frac{62 \times 9.1}{62 + 9.1} = 7.94\,\text{k}\Omega$$

and, using the voltage divider rule, an equivalent voltage source such that

$$E_{\text{th}} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{9.1 \times 16}{62 + 9.1} = 2.05\ \text{V}$$

Once the Thévenin equivalent resistance and voltage source have been established, the analysis becomes no different from that of an emitter-bias configuration. To determine the base current I_B, we write

$$E_{\text{th}} - I_B R_{\text{th}} - V_{BE} - I_E R_E = 0 \rightarrow E_{\text{th}} - I_B R_{\text{th}} - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$\therefore I_{B_Q} = \frac{E_{\text{th}} - V_{BE}}{R_{\text{th}} + (\beta + 1) R_E} = \frac{2.05 - 0.7}{7.94 + (80 + 1) \times 0.68} = 0.0214\,\text{mA} = \boxed{21.4\,\mu\text{A}}$$

Notice that the formula for I_{B_Q} would be identical to the one used in Problem 8 had we replaced E_{th} with V_{CC} and R_{th} with R_B.

To determine the collector current, simply multiply I_{B_Q} by the BJT's current gain parameter β = 80,

$$I_{C_Q} = \beta I_{B_Q} = 80 \times 0.0214 = \boxed{1.71\,\text{mA}}$$

V_{CE} can be determined by applying KVL to the collector-emitter junction; the ensuing formula is identical to the one obtained for the emitter-bias configuration of Problem 8,

$$V_{CE} = V_{CC} - I_C (R_C + R_E) = 16 - 1.71 \times (3.9 + 0.68) = \boxed{8.17\,\text{V}}$$

The collector-to-ground voltage is given by

$$V_C = V_{CE} + \underbrace{I_E}_{=I_C} R_E = V_{CE} + I_C R_E = 8.17 + 1.71 \times 0.68 = \boxed{9.33\,\text{V}}$$

The emitter-to-ground voltage is given by $V_E = I_E R_E$; since the base current is substantially less than the other two current components, we may use the approximation $I_E \approx I_C$ and write

$$V_E = I_E R_E \approx I_C R_E = 1.71 \times 0.68 = \boxed{1.16\,\text{V}}$$

The base voltage is given by

$$V_B = V_E + V_{BE} = 1.16 + 0.7 = \boxed{1.86\,\text{V}}$$

P.12 ➡ *Solution*

Note that the collector resistance is positioned between the supply voltage node V_{CC} = 18 V and the collector node V_C = 12 V; using this information, the collector current is found as

$$V_{CC} - I_C R_C = V_C \rightarrow I_C = \frac{V_{CC} - V_C}{R_C}$$

$$\therefore I_C = \frac{18-12}{4.7} = \boxed{1.28\,\text{mA}}$$

Assuming $I_E \approx I_C$, the emitter voltage is determined to be

$$V_E = I_E R_E \approx I_C R_E = 1.28 \times 1.2 = \boxed{1.54\,\text{V}}$$

The base-to-ground voltage can be determined from the definition of V_{BE},

$$V_{BE} = V_B - V_E \rightarrow V_B = V_{BE} + V_E$$
$$\therefore V_B = 0.7 + 1.54 = \boxed{2.24\,\text{V}}$$

Applying KVL one last time gives resistance R_1,

$$V_{CC} - I_{R_1} R_1 = V_B \rightarrow R_1 = \frac{V_{CC} - V_B}{I_{R_1}}$$

The current through resistor R_1 is missing; one reasonable assumption is to equate it to the current through R_2, which is calculated as

$$I_{R_2} = \frac{V_B}{R_2} = \frac{2.24}{5.6} = 0.4\,\text{mA}$$

so that

$$R_1 = \frac{V_{CC} - V_B}{\underbrace{I_{R_1}}_{\approx I_{R_2}}} = \frac{18 - 2.24}{0.4} = \boxed{39.4\,\text{k}\Omega}$$

P.13 ➡ *Solution*

In principle, we could determine the collector current by applying KVL to the collector branch of the circuit; however, this requires the supply voltage V_{CC}, which is missing. A second possibility is to use the base current I_B = 20 μA and the BJT's current gain parameter β; mathematically,

$$\beta = \frac{I_C}{I_B} \rightarrow I_C = \beta I_B$$

$$\therefore I_C = 100 \times \left(20 \times 10^{-6}\right) = \boxed{2.0\,\text{mA}}$$

To determine emitter voltage V_E, we apply Ohm's law to the emitter branch of the circuit,

$$V_E = \underbrace{I_E}_{\approx I_C} R_E = 2.0 \times 1.2 = \boxed{2.4\,\text{V}}$$

Applying KVL to the collector branch of the circuit gives V_{CC},

$$V_{CC} - I_C R_C = V_C \rightarrow V_{CC} = V_C + I_C R_C$$
$$\therefore V_{CC} = 10.6 + 2.0 \times 2.7 = \boxed{16\,\text{V}}$$

With V_C = 10.6 V and V_E = 2.4 V, calculating the collector-emitter voltage couldn't be any easier,

$$V_{CE} = V_C - V_E = 10.6 - 2.4 = \boxed{8.2\,\text{V}}$$

The base voltage is

$$V_{BE} = V_B - V_E \rightarrow V_B = V_{BE} + V_E$$
$$\therefore V_B = 0.7 + 2.4 = \boxed{3.1\,\text{V}}$$

To determine resistance R_1, we first apply Kirchhoff's current law to determine the current flowing through it,

$$I_{R_1} = I_{R_2} + I_B = \frac{3.1}{8.2} + 0.02 = 0.398\,\text{mA}$$

so that

$$V_{CC} - I_{R_1} R_1 = V_B \rightarrow R_1 = \frac{V_{CC} - V_B}{I_{R_1}}$$
$$\therefore R_1 = \frac{16 - 3.1}{0.398} = \boxed{32.4\,\text{k}\Omega}$$

P.14 ➡ *Solution*

We essentially have two voltage-divider bias networks with a common voltage source of 20 V. The base voltage of Q_1 can be obtained in approximate fashion with the voltage-divider rule,

$$V_B \approx \frac{4.7\times 20}{18+4.7} = \boxed{4.14\,\text{V}}$$

Next, noting that $V_{BE} = 0.7$ V,

$$V_{BE} = V_B - V_E \rightarrow V_E = V_B - V_{BE}$$
$$\therefore V_E = 4.14 - 0.7 = \boxed{3.44\,\text{V}}$$

Applyng Ohm's law to the emitter branch of Q_1 brings to

$$V_E = I_E R_E \rightarrow I_E = \frac{V_E}{R_E} = \frac{3.44}{1.0} = 3.44\,\text{mA}$$

so that, for the collector branch,

$$I_C = \left(\frac{\beta}{\beta+1}\right) I_E = \left(\frac{160}{160+1}\right)\times 3.44 = 3.42\,\text{mA}$$

giving

$$V_C = V_{CC} - I_C R_C = 20 - 3.42\times 2.2 = \boxed{12.48\,\text{V}}$$

Notice that we have already determined I_E and I_C. To compute the base current, use one of the current gain parameter relations or, better yet, simply write

$$I_C + I_B = I_E \rightarrow I_B = I_E - I_C$$
$$\therefore I_B = 3.44 - 3.42 = 0.02\,\text{mA} = \boxed{20\,\mu\text{A}}$$

Also,

$$\boxed{I_C = 3.42\,\text{mA}}$$

$$\boxed{I_E = 3.44\,\text{mA}}$$

Calculations for transistor Q_2 are identical to those for Q_1.

$$V_{B,2} = \frac{3.3\times 20}{22+3.3} = \boxed{2.61\,\text{V}}$$
$$V_E = V_B - V_{BE}$$
$$\therefore V_{E,2} = 2.61 - 0.7 = \boxed{1.91\,\text{V}}$$
$$I_{E,2} = \frac{V_E}{R_E} = \frac{1.91}{1.2} = \boxed{1.59\,\text{mA}}$$
$$I_{C,2} = \left(\frac{\beta}{\beta+1}\right) I_E = \left(\frac{90}{90+1}\right)\times 1.59 = \boxed{1.57\,\text{mA}}$$
$$V_{C,2} = V_{CC} - I_C R_C = 20 - 3.40\times 2.2 = \boxed{12.52\,\text{V}}$$
$$I_{B,2} = \frac{I_C}{\beta} = \frac{1.57}{90} = 0.0174\,\text{mA} = \boxed{17.4\,\mu\text{A}}$$

P.15 ➡ *Solution*

Applying Kirchhoff's voltage law to the sequence voltage source → collector → feedback loop → emitter, we obtain

$$V_{CC} - \underbrace{\left(I_C + I_B\right)}_{\approx I_C} R_C - I_B R_F - V_{BE} - I_E R_E = 0$$
$$\therefore V_{CC} - \underbrace{I_C}_{=\beta I_B} R_C - I_B R_F - V_{BE} - \underbrace{I_E}_{\approx I_C} R_E = 0$$
$$\therefore V_{CC} - \beta I_B R_C - I_B R_F - V_{BE} - I_C R_E = 0$$
$$\therefore V_{CC} - \beta I_B R_C - I_B R_F - V_{BE} - \beta I_B R_E = 0$$
$$\therefore V_{CC} - V_{BE} = \beta I_B R_C + I_B R_F + \beta I_B R_E$$
$$\therefore V_{CC} - V_{BE} = I_B \times \left[R_F + \beta\left(R_C + R_E\right)\right]$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)} = \frac{16 - 0.7}{270 + 120 \times (3.6 + 1.2)} = 0.0181\,\text{mA} = \boxed{18.1\,\mu\text{A}}$$

The collector current is

$$I_C = \beta I_B = 120 \times 0.0181 = \boxed{2.17\,\text{mA}}$$

Applying KVL to the circuit branch stemming from the voltage source node, we obtain

$$V_{CC} - I_C R_C = V_C \rightarrow V_C = 16 - 2.17 \times 3.6 = \boxed{8.19\,\text{V}}$$

P.16 ➡ Solution

Suppose first that the potentiometer in the feedback loop offers zero additional resistance to the circuit. In this case, $R_F = 150 + 0 = 150$ kΩ and, using the formula derived in Problem 15, the base current is

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)} = \frac{12 - 0.7}{(150 + 0) + 180 \times (4.7 + 3.3)} = 0.00711\,\text{mA} = 7.11\,\mu\text{A}$$

so that, from the definition of current gain parameter β,

$$\beta = \frac{I_C}{I_B} \rightarrow I_C = \beta I_B$$

$$\therefore I_C = 180 \times 0.00711 = 1.28\,\text{mA}$$

Then, applying KVL to the collector branch of the circuit, voltage V_C is calculated to be

$$V_{CC} - I_C R_C = V_C \rightarrow V_C = 12 - 1.28 \times 4.7 = \boxed{5.98\,\text{V}}$$

Assume now that the potentiometer is set to its maximum rating of 1 MΩ, so that $R_F = 150 + 1000 = 1150$ kΩ. The base current is updated as

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)} = \frac{12 - 0.7}{(150 + 1000) + 180 \times (4.7 + 3.3)} = 0.00436\,\text{mA} = 4.36\,\mu\text{A}$$

and the collector current becomes

$$I_C = 180 \times 0.00436 = 0.785\,\text{mA}$$

giving a new collector voltage V_C such that

$$V_C = 12 - 0.785 \times 4.7 = \boxed{8.31\,\text{V}}$$

Thus, as the potentiometer resistance varies from zero to 1 MΩ, the collector-to-ground voltage changes from 5.98 V to 8.31 V.

P.17 ➡ Solution

Using $V_{BE} = 0.7$ V, the emitter-to-ground voltage is found as

$$V_{BE} = V_B - V_E \rightarrow V_E = V_B - V_{BE}$$

$$\therefore V_E = 4 - 0.7 = \boxed{3.3\,\text{V}}$$

The collector current is approximately equal to the emitter current, and I_C can be determined by applying Ohm's law to the emitter branch of the circuit,

$$V_E = I_E R_E \approx I_C R_E \rightarrow I_C \approx \frac{V_E}{R_E}$$

$$\therefore I_C = \frac{3.3}{1.2} = \boxed{2.75\,\text{mA}}$$

Applying KVL to the collector branch of the circuit should yield the collector voltage V_C,

$$V_C = V_{CC} - I_C R_C = 18 - 2.75 \times 2.2 = \boxed{11.95\,\text{V}}$$

Gleaning the values of V_E and V_C, we may write

$$V_{CE} = V_C - V_E = 11.95 - 3.3 = \boxed{8.65\,\text{V}}$$

The base current can be determined as

$$V_C - I_B R_F = V_B \rightarrow I_B = \frac{V_C - V_B}{R_F}$$

$$\therefore I_B = \frac{11.95-4}{330} = 0.0241\,\text{mA} = \boxed{24.1\,\mu\text{A}}$$

Gathering the values of I_C and I_B, we write

$$\beta = \frac{I_C}{I_B} = \frac{2.75}{0.0241} = \boxed{114}$$

P.18 ➡ Solution

A simple way to determine the base current in a common-base configuration is to first establish the emitter current I_E, then use the BJT's current gain parameter to compute I_B. Proceeding in this manner, we write, for the emitter junction,

$$V_{EE} - I_E R_E = V_{BE} \rightarrow I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$\therefore I_E = \frac{12-0.7}{15} = 0.753\,\text{mA}$$

so that

$$I_E = (1+\beta) I_B \rightarrow I_B = \frac{I_E}{1+\beta}$$

$$\therefore I_B = \frac{0.753}{1+80} = 0.00930\,\text{mA} = \boxed{9.30\,\mu\text{A}}$$

Equipped with I_E and I_B, we can determine the remaining current component,

$$I_E = I_C + I_B \rightarrow I_C = I_E - I_B$$

$$\therefore I_C = 0.753 - 0.00930 = \boxed{0.744\,\text{mA}}$$

To determine the collector-emitter voltage, we apply KVL to, you guessed it, the collector-emitter junction,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E + V_{EE} = 0$$

$$\therefore V_{CE} = V_{CC} - I_C R_C - I_E R_E + V_{EE}$$

$$\therefore V_{CE} = 16 - 0.744 \times 12 - 0.753 \times 15 + 12 = \boxed{7.77\,\text{V}}$$

Applying KVL one last time gives the collector-to-ground voltage V_C,

$$V_C = V_{CC} - I_C R_C = 16 - 0.744 \times 12 = \boxed{7.07\,\text{V}}$$

P.19 ➡ Solution

Applying KVL to the emitter branch brings to

$$V_{EE} - I_E R_E = V_{BE} \rightarrow I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$\therefore I_E = \frac{8-0.7}{2.2} = \boxed{3.32\,\text{mA}}$$

Let $I_C \approx I_E = 3.95$ mA. Applying KVL to the collector branch, we obtain

$$V_C = V_{CC} - \underbrace{I_C}_{\approx I_E} R_C = 10 - 3.32 \times 1.8 = \boxed{4.02\,\text{V}}$$

Considering the entire collector-emitter junction and making use of $I_C \approx I_E$, we get

$$V_{CC} - \underbrace{I_C}_{\approx I_E} R_C - V_{CE} - I_E R_E + V_{EE} = 0$$

$$\therefore V_{CE} = V_{CC} + V_{EE} - I_E (R_C + R_E) = 10 + 8 - 3.32 \times (1.8 + 2.2) = \boxed{4.72\,\text{V}}$$

P.20 ➡ Solution

We first determine the emitter voltage V_E,

$$V_{BE} = V_B - V_E \rightarrow V_E = V_B - V_{BE}$$

$$\therefore V_E = 4.0 - 0.7 = 3.3\,\text{V}$$

Then, we compute the emitter current I_E,

$$V_E = I_E R_E \rightarrow I_E = \frac{V_E}{R_E}$$

$$\therefore I_E = \frac{3.3}{1.1} = \boxed{3\,\text{mA}}$$

The corresponding collector current is

$$I_C = \left(\frac{\beta}{1+\beta}\right) I_E = \left(\frac{90}{1+90}\right) \times 3 = 2.97\,\text{mA}$$

and can be used to establish the value of resistance R_C,

$$V_{CC} - I_C R_C = V_C \rightarrow R_C = \frac{V_{CC} - V_C}{I_C}$$

$$\therefore R_C = \frac{14-8}{2.97} = \boxed{2.02\,\text{k}\Omega}$$

Using I_E and I_C = 2.97 mA clearly gives, for the base current I_B,

$$I_C + I_B = I_E \rightarrow I_B = I_E - I_C$$

$$\therefore I_B = 3 - 2.97 = 0.03\,\text{mA} = \boxed{30\,\mu\text{A}}$$

Given V_B = 4 V and V_C = 8 V, the base-collector voltage is calculated to be

$$V_{BC} = V_B - V_C = 4 - 8 = \boxed{-4\,\text{V}}$$

We already established that V_E = 3.3 V; also, V_C = 8 V. The collector-emitter voltage is then

$$V_{CE} = V_C - V_E = 8 - 3.3 = \boxed{4.7\,\text{V}}$$

P.21 ➡ *Solution*

We first determine the base current I_B,

$$V_{CC} - I_B R_B = V_B \rightarrow I_B = \frac{V_{CC} - V_B}{R_B}$$

$$\therefore I_B = \frac{V_{CC} - V_B}{R_B} = \frac{V_{CC} - (V_{BE} + V_E)}{R_B} = \frac{12 - (0.7 + 0)}{510} = 0.0222\,\text{mA} = 22.2\,\mu\text{A}$$

Then, using the current gain parameter β, we compute collector current I_C,

$$\beta = \frac{I_C}{I_B} \rightarrow I_C = \beta I_B$$

$$\therefore I_C = 100 \times 0.0222 = \boxed{2.22\,\text{mA}}$$

Applying KVL to the collector junction should yield voltage V_C,

$$V_C = -V_{CC} + I_C R_C = -12 + 2.22 \times 3.3 = \boxed{-4.67\ \text{V}}$$

Lastly, V_{CE} is

$$V_{CE} = V_C - \underbrace{V_E}_{=0} = V_C = \boxed{-4.67\ \text{V}}$$

P.22 ➡ *Solution*

For the approximate approach to be valid, we must have

$$\beta R_E \geq 10 R_2 \rightarrow 220 \times 0.75 \left\langle ? \right\rangle 10 \times 16$$

$$165 > 160 \ (\text{Checks!})$$

Using the approximate approach, the base voltage can be established as

$$V_B \approx \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{16 \times (-22)}{82 + 16} = -3.59\,\text{V}$$

so that

$$V_{BE} = V_B - V_E \rightarrow V_E = V_B - V_{BE}$$

$$\therefore V_E = -3.59 - (-0.7) = -2.89\,\text{V}$$

Using this voltage, we can determine the emitter current I_E,

$$V_E = I_E R_E \rightarrow I_E = \frac{V_E}{R_E}$$

$$\therefore I_E = \frac{2.89}{0.75} = 3.85\,\text{mA}$$

With $I_C \approx I_E$, applying KVL to the collector junction brings to

$$V_C = -V_{CC} + \underbrace{I_C}_{\approx I_E} R_C = -22 + 3.85 \times 2.2 = \boxed{-13.53\ \text{V}}$$

Lastly, with a current gain parameter $\beta = 220$,

$$I_B = \frac{I_C}{\beta} = \frac{3.85}{220} = 0.0175\,\text{mA} = \boxed{17.5\,\mu\text{A}}$$

P.23 ➡ Solution

Applying KVL to the emitter branch brings to

$$V_{EE} - I_E R_E = V_{BE} \rightarrow I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$\therefore I_E = \frac{8 - 0.7}{3.3} = \boxed{2.21\,\text{mA}}$$

Using $I_C \approx I_E$, the collector voltage is calculated to be

$$V_C = -V_{CC} + \underbrace{I_C}_{\approx I_E} R_C = -12 + 2.21 \times 3.9 = \boxed{-3.38\,\text{V}}$$

P.24 ➡ Solution

Problem 24.1: First note that $V_{DS} = 6$ V and $V_{GS} - V_{TN} = 5 - 1.5 = 3.5$ V; since $V_{DS} > V_{GS} - V_{TN}$, the FET is biased in the saturation region and the drain current is given by

$$I_D = K_n \left(V_{GS} - V_{TN}\right)^2 = 0.25 \times \left(5.0 - 1.5\right)^2 = \boxed{3.06\ \text{mA}}$$

Problem 24.2: In this case, $V_{DS} = 2.5$ V and $V_{GS} - V_{TN} = 5 - 1.5 = 3.5$ V; since $V_{DS} < V_{GS} - V_{TN}$, the FET is biased in the nonsaturation region and the drain current is given by

$$I_D = K_n \left[2\left(V_{GS} - V_{TN}\right)V_{DS} - V_{DS}^2\right] = 0.25\left[2 \times \left(5.0 - 1.5\right) \times 2.5 - 2.5^2\right] = \boxed{2.81\,\text{mA}}$$

P.25 ➡ Solution

Evoking the equation for drain current in the saturation region and solving for V_{GS}, we obtain

$$I_D = K_n \left(V_{GS} - V_{TN}\right)^2 \rightarrow \sqrt{\frac{I_D}{K_n}} = V_{GS} - V_{TN}$$

$$\therefore V_{GS} = \sqrt{\frac{I_D}{K_n}} + V_{TN} = \sqrt{\frac{I_D}{k_n' W/(2L)}} + V_{TN}$$

$$\therefore V_{GS} = \sqrt{\frac{0.5}{0.08 \times 5/2}} + 0.8 = \boxed{2.38\,\text{V}}$$

The corresponding saturation drain-source voltage is

$$V_{DS}\,(\text{sat}) = V_{GS} - V_{TN} = 2.38 - 0.8 = \boxed{1.58\,\text{V}}$$

P.26 ➡ Solution

Problem 26.1: The MOSFET conduction parameter K_n is expressed as

$$K_n = \frac{k_n' W}{2L} \quad \text{(I)}$$

where the process conduction parameter k_n' equals the product of electron mobility and oxide-layer capacitance:

$$k_n' = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}} = \frac{650 \times \left[3.9 \times \left(8.85 \times 10^{-14}\right)\right]}{450 \times 10^{-8}} = 4.99 \times 10^{-5}\ \text{A/V}^2$$

Substituting in (I), we obtain

$$K_n = \frac{k_n' W}{2L} = \frac{\left(4.99\times10^{-5}\right)\times 64}{2\times 4} = 3.99\times10^{-4}\ \text{A/V}^2 = \boxed{0.399\,\text{mA/V}^2}$$

Problem 26.2: With $V_{GS} = V_{DS} = 3$ V, the FET is operating in saturation; accordingly, its drain current can be determined with the equation

$$I_D = K_n\left(V_{GS} - V_{TN}\right)^2 = 0.399\times\left(3-0.8\right)^2 = \boxed{1.93\,\text{mA}}$$

P.27 ➡ Solution

If the device is operating in the saturation region, the drain current is given by

$$I_D = K_n\left(V_{GS} - V_{TN}\right)^2 \quad \text{(I)}$$

The MOSFET conduction parameter can be expanded as

$$K_n = \frac{k_n' W}{2L} = \frac{\mu_n C_{ox} W}{2L} = \frac{\mu_n \varepsilon_{ox} W}{2t_{ox} L}$$

$$\therefore K_n = \frac{600\times\left[3.9\times\left(8.85\times10^{-14}\right)\right]\times W}{2\times\left(400\times10^{-8}\right)\times\left(2.5\times10^{-4}\right)} = 0.104W$$

so that, substituting in (I) and solving for W,

$$I_D = K_n\left(V_{GS} - V_{TN}\right)^2 \rightarrow I_D = 0.104W\times\left(V_{GS} - V_{TN}\right)^2$$

$$\therefore W = \frac{I_D}{0.104\left(V_{GS} - V_{TN}\right)^2} = \frac{1.2\times10^{-3}}{0.104\times\left(5.0-1.0\right)^2} = 7.21\times10^{-4}\ \text{cm} = \boxed{7.21\,\mu\text{m}}$$

P.28 ➡ Solution

Since this is a p-channel FET, the saturation source-drain voltage can be stated as

$$V_{SD}\left(\text{sat}\right) = V_{SG} + V_{TP} = 0 + 2 = 2\,\text{V}$$

Now, with $V_{SD} = 1\ \text{V} < V_{SD}(sat)$, the FET is operating in nonsaturation and the drain current can be determined as

$$I_D = K_p\left[2\left(V_{SG} + V_{TP}\right)V_{SD} - V_{SD}^2\right] = 0.5\times\left[2.0\times\left(0+2.0\right)\times1.0 - 1.0^2\right] = \boxed{1.5\,\text{mA}}$$

Next, with $V_{SD} = 2\ \text{V} = V_{SD}(sat)$, the FET is operating in saturation and the drain current is given by

$$I_D = K_p\left(V_{SG} + V_{TP}\right)^2 = 0.5\times\left(0+2.0\right)^2 = \boxed{2\,\text{mA}}$$

Lastly, with $V_{SD} = 3\ \text{V} > V_{SD}(sat)$, the FET is in saturation and conducts the same drain current as when $V_{SD} = 2$ V,

$$\boxed{I_D = 2\,\text{mA}}$$

P.29 ➡ Solution

Since both devices have the same oxide thickness $t_{ox} = 500$ Å, they share a common oxide-layer capacitance C_{ox} such that

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9\times\left(8.85\times10^{-14}\right)}{500\times10^{-8}} = 6.90\times10^{-8}\ \text{F/cm}^2$$

The process conduction parameter for the NMOS is

$$k_n' = \mu_n C_{ox} = 675\times\left(6.90\times10^{-8}\right) = 4.66\times10^{-5}\ \text{A/V}^2$$

while, for the PMOS,

$$k_p' = \mu_p C_{ox} = 375\times\left(6.90\times10^{-8}\right) = 2.59\times10^{-5}\ \text{A/V}^2$$

Now, if the PMOS is to conduct a drain current of 0.8 mA when subjected to a source-gate voltage of 5 V, we may write the following and solve for aspect ratio,

$$I_D = \frac{k_p'}{2}\left(\frac{W}{L}\right)_p\left(V_{SG} + V_{TP}\right)^2 \rightarrow \left(\frac{W}{L}\right)_p = \frac{2I_D}{k_p'\left(V_{SG} + V_{TP}\right)^2}$$

$$\therefore \left(\frac{W}{L}\right)_p = \frac{2\times\left(0.8\times10^{-3}\right)}{\left(2.59\times10^{-5}\right)\times\left(5-0.6\right)^2} = 3.19$$

Since channel length L = 4 μm,

$$W_p = 3.19L_p = 3.19\times4 = \boxed{12.8\ \mu\text{m}}$$

We can also determine the PMOS conduction parameter,

$$K_p = \frac{k_p'}{2}\left(\frac{W}{L}\right)_p = \frac{\left(2.59\times10^{-5}\right)}{2}\times3.19 = 4.13\times10^{-5}\ \text{A/V}^2 = \boxed{41.3\,\mu\text{A/V}^2}$$

For the two transistors to be electrically equivalent, the conduction parameter of the NMOS must be equal to that of the PMOS; that is,

$$K_n = K_p = \boxed{41.3\,\mu\text{A/V}^2}$$

Using this relationship, we can determine the aspect ratio of the NMOS,

$$K_n = K_p \rightarrow \frac{k_n'}{2}\left(\frac{W}{L}\right)_n = \frac{k_p'}{2}\left(\frac{W}{L}\right)_p$$

$$\therefore \frac{4.66\times10^{-5}}{\cancel{2}}\left(\frac{W}{L}\right)_n = \frac{2.59\times10^{-5}}{\cancel{2}}\underbrace{\left(\frac{W}{L}\right)_p}_{=3.19}$$

$$\therefore \left(\frac{W}{L}\right)_n = \frac{2.59\times10^{-5}}{4.66\times10^{-5}}\times3.19 = 1.77$$

Finally, with L = 4 μm,

$$W_n = 1.77L = 1.77\times4 = \boxed{7.08\ \mu\text{m}}$$

In summary, the devices will be electrically equivalent if they are designed such that $K_n = K_p$ = 41.3 μA/V², W_n = 7.08 μm, and W_p = 12.8 μm.

P.30 ➡ Solution

WIth I_{DSS} = 12 mA and V_P = −4 V, Shockley's equation for this device can be written as

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = 12\times\left[1-\frac{V_{GS}}{(-4)}\right]^2$$

Folowing Boylestad and Nashelsky, we plot the transfer curve with four reference V_{GS} values, namely 0 V, $V_{GS} = V_P$ = −4 V, $V_p/2$ = −2 V, and $0.3V_P$ = −1.2 V. The corresponding I_D values are tabulated below.

V_{GS}	I_D
0 V	12 mA
−4 V	0 mA
$V_P/2 = -4/2 = -2$ V	$12\times[1-(-2)/(-4)]^2 = 3$ mA
$0.3V_P = 0.3\times(-4) = -1.2$ V	$12\times[1-(-1.2)/(-4)]^2 = 5.88$ mA

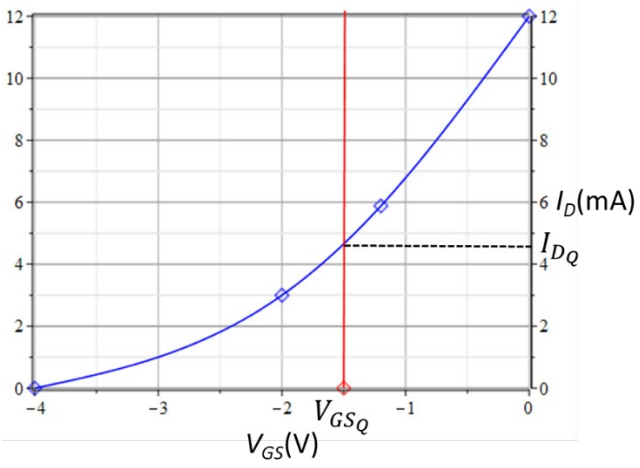
The transfer curve can be plotted with these four points. The Q-point coordinates are found by superimposing the transfer curve with the fixed-bias line, which in turn can be defined if we apply Kirchhoff's voltage law to the gate-source junction of the network:

$$-V_{GG} - V_{GS} = 0 \rightarrow V_{GS} = -V_{GG}$$

But V_{GG} = 1.5 V, so

$$V_{GS} = -1.5$$

Recall from your knowledge of analytic geometry that an expression of the type $x = const.$ plots as a vertical line on the xy-plane. Analogously, V_{GS} = −1.5 V represents a vertical line on the V_{GS}-I_D plane and intercepts the voltage axis at (−1.5, 0). The transfer curve and the load line in question are shown below. By inspection, we see that the quiescent gate-source voltage is V_{GS_Q} = −1.5 V (obviously), while the quiescent drain current is $I_{D_Q} \approx$ 4.8 mA.



Applying Kirchhoff's voltage law to the drain branch of the network, we can determine the quiescent drain-source voltage,

$$V_{DS_Q} = V_{DD} - I_{D_Q} R_D = 14 - 4.8 \times 1.8 = \boxed{5.36\,\text{V}}$$

To determine I_{D_Q} mathematically, simply substitute $V_{GS} = V_{GS_Q} = -1.5$ V in Shockley's equation, giving

$$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2 = 12 \times \left[1 - \frac{(-1.5)}{-4}\right]^2 = \boxed{4.69\,\text{mA}}$$

There is good agreement between this result and the graphical estimate $I_{D_Q} = 4.8$ mA. The corresponding V_{DS_Q} is

$$V_{DS_Q} = V_{DD} - I_{D_Q} R_D = 14 - 4.69 \times 1.8 = \boxed{5.56\,\text{V}}$$

P.31 ➡ *Solution*

WIth $I_{DSS} = 10$ mA and $V_P = -4$ V, Shockley's equation for this device reads

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10 \times \left[1 - \frac{V_{GS}}{(-4)}\right]^2$$

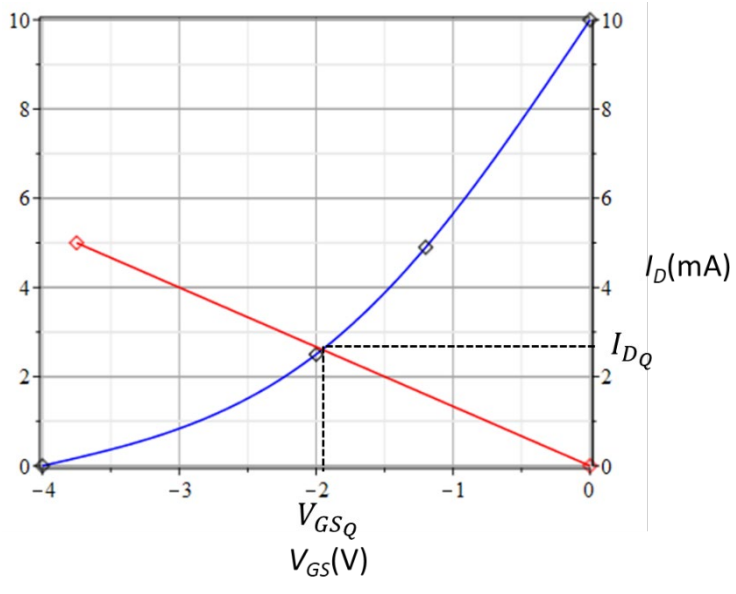
Drain currents for four typical values of V_{GS} are tabulated below.

V_{GS}	I_D
0 V	10 mA
−4 V	0 mA
$V_P/2 = -4/2 = -2$ V	$10 \times [1 - (-2)/(-4)]^2 = 2.5$ mA
$0.3V_P = 0.3 \times (-4) = -1.2$ V	$10 \times [1 - (-1.2)/(-4)]^2 = 4.9$ mA

The points above define the transfer curve. The second step is to draw the self-bias line, which is defined by the simple relation $V_{GS} = -I_D R_S$, with $R_S = 0.75$ kΩ. The first obvious point choice is the origin itself, because if $I_D = 0$ then $V_{GS} = -0 \times 0.75 = 0$ V. For the second point, let us take $I_D = I_{DSS}/2 = 10/2$ mA, giving

$$V_{GS} = -I_D R_S = -\frac{I_{DSS} R_S}{2} = -\frac{10 \times 0.75}{2} = -3.75\,\text{V}$$

Thus, the self-bias line is defined by points (0,0) and (−3.75, 5). This line is superposed to the transfer curve in the following graph. By inspection, we see that $I_{D_Q} \approx 2.6$ mA and $V_{GS_Q} \approx -1.95$ V.



Using the quiescent drain current determined above, the drain-source voltage is calculated to be

$$V_{DS} = V_{DD} - I_D\left(R_D + R_S\right) = 18 - 2.6\times\left(1.5 + 0.75\right) = \boxed{12.15\ \text{V}}$$

The drain voltage V_D is, in turn,

$$V_D = V_{DD} - I_D R_D = 18 - 2.6\times 1.5 = \boxed{14.1\,\text{V}}$$

The gate voltage V_G in a self-bias configuration equals zero:

$$\boxed{V_G = 0\,\text{V}}$$

Using V_{DS} = 12.15 V and V_D = 14.1 V, we can establish the source voltage V_S,

$$V_{DS} = V_D - V_S \rightarrow V_S = V_D - V_{DS}$$

$$\therefore V_S = 14.1 - 12.15 = \boxed{1.95\,\text{V}}$$

Notice that $V_S \approx |V_{GS}|$.

In a purely mathematical treatment, substitute $V_{GS} = -I_D R_S$ into Shockley's equation and expand, giving

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left[1 - \frac{\left(-I_D R_S\right)}{V_P}\right]^2 = \frac{I_{DSS}R_S^2}{V_P^2}I_D^2 + \frac{2I_{DSS}R_S}{V_P}I_D + I_{DSS}$$

$$\therefore \frac{I_{DSS}R_S^2}{V_P^2}I_D^2 + \left(\frac{2I_{DSS}R_S}{V_P} - 1\right)I_D + I_{DSS}$$

$$\therefore \frac{\left(10\times10^{-3}\right)\times 750^2}{\left(-4\right)^2}I_D^2 + \left[\frac{2\times\left(10\times10^{-3}\right)\times 750}{\left(-4\right)} - 1\right]I_D + 10\times10^{-3} = 0$$

$$\therefore 352 I_D^2 - 4.75 I_D + 0.01 = 0$$

$$\therefore I_{D_Q} = \left[\frac{4.75 \pm \sqrt{\left(-4.75\right)^2 - 4\times352\times0.01}}{2\times352}\right]\times10^3 = \cancel{10.88\,\text{mA}},\ \boxed{2.61\,\text{mA}}$$

The corresponding V_{GS} is

$$V_{GS_Q} = -I_{D_Q}R_S = -2.61\times0.75 = \boxed{1.96\,\text{V}}$$

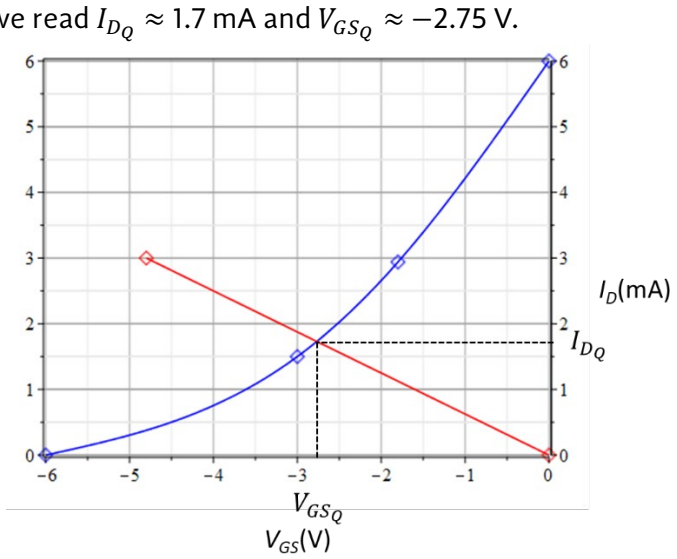
There is excellent agreement between the graphical method and the purely mathematical approach.

P.32 ➡ *Solution*

We proceed in much the same way as in Problem 31. First, we tabulate four V_{GS}-I_D data points:

V_{GS}	I_D
0 V	6 mA
−6 V	0 mA
$V_P/2 = -6/2 = -3$ V	$6 \times [1 - (-3)/(-6)]^2 = 1.5$ mA
$0.3V_P = 0.3 \times (-6) = -1.8$ V	$10 \times [1 - (-1.8)/(-6)]^2 = 2.94$ mA

Now, the self-bias line is defined by $V_{GS} = -I_D R_S$; one point is (0,0), and another can be obtained by taking, say, $I_D = I_{SS}/2 = 6/2 = 3$ mA, so that $V_{GS} = -3 \times 1.6 = -4.8$ V. The transfer curve and self-bias line are superposed below. By inspection, we read $I_{D_Q} \approx 1.7$ mA and $V_{GS_Q} \approx -2.75$ V.



Using the quiescent drain current determined above, the drain-source voltage is computed as

$$V_{DS} = V_{DD} - I_D\left(R_D + R_S\right) = 12 - 1.7 \times \left(2.2 + 1.6\right) = \boxed{5.54\ \text{V}}$$

The drain voltage V_D is, in turn,

$$V_D = V_{DD} - I_D R_D = 12 - 1.7 \times 2.2 = \boxed{8.26\,\text{V}}$$

The gate voltage V_G in a self-bias configuration equals zero:

$$\boxed{V_G = 0\,\text{V}}$$

Using V_{DS} = 5.54 V and V_D = 8.26 V, we can establish the source voltage V_S,

$$V_{DS} = V_D - V_S \rightarrow V_S = V_D - V_{DS}$$
$$\therefore V_S = 8.26 - 5.54 = \boxed{2.72\,\text{V}}$$

Notice that $V_S \approx |V_{GS}|$.

P.33 ➡ *Solution*

In the present case, a simple way to determine I_{D_Q} is to refer to the source branch, for which we have the measurement V_S = 1.7 V, and use $I_{D_Q} \approx I_S$:

$$I_{D_Q} = I_S = \frac{V_S}{R_S} = \frac{1.7}{0.51} = \boxed{3.33\,\text{mA}}$$

In a self-bias configuration, $V_{GS_Q} = -I_{D_Q} R_S$, so that

$$V_{GS_Q} = -I_{D_Q} R_S = -3.33 \times 0.51 = \boxed{-1.70\,\text{V}}$$

To determine the maximum current, substitute any of the transfer curve's (V_{GS}, I_D) pairs into Shockley's equation and solve for I_{DSS}; an obvious choice here is the Q-point itself:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \rightarrow I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2$$

$$\therefore I_{DSS} = \frac{I_{D_Q}}{\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2} = \frac{3.33}{\left[1 - \frac{(-1.70)}{-4}\right]^2} = \boxed{10.07\,\text{mA}}$$

The drain voltage is

$$V_D = V_{DD} - I_D R_D = 18 - 3.33 \times 2 = \boxed{11.34\,\text{V}}$$

Using the value of V_D determined above and the given V_S, we can easily determine the drain-source voltage:

$$V_{DS} = V_D - V_S = 11.34 - 1.7 = \boxed{9.64\,\text{V}}$$

P.34 ➡ *Solution*

Since the gate and source are shorted, $V_G = V_S$ and

$$V_{GS} = V_G - V_S = 0\,\text{V}$$

With V_{GS} = 0 V, Shockley's equation gives

$$I_D = I_{DSS}\left(1 - \frac{\underbrace{V_{GS}}_{=0}}{V_P}\right)^2 = I_{DSS} \times \left(1 - \frac{0}{-5}\right)^2 = I_{DSS} = \boxed{4.5\,\text{mA}}$$

Applying Kirchhoff's voltage law to the drain region, we get

$$V_{DS} = V_{DD} + V_{SS} - I_D\left(R_D + R_S\right) = \left(20 + 4\right) - 4.5 \times \left(2.2 + 0.68\right) = \boxed{11.04\,\text{V}}$$

Applying KVL a second time yields

$$V_D = V_{DD} - I_D R_D = 20 - 4.5 \times 2.2 = \boxed{10.1\,\text{V}}$$

With V_{DS} and V_D, the source-to-ground voltage is found as

$$V_{DS} = V_D - V_S \rightarrow V_S = V_D - V_{DS}$$
$$\therefore V_S = 10.1 - 11.04 = \boxed{-0.94\ \text{V}}$$

P.35 ➡ *Solution*

Problem 35.1: The gate-to-ground voltage can be determined with the voltage divider rule,

$$V_G = \frac{110 \times 20}{110 + 910} = \boxed{2.16\ \text{V}}$$

To establish the *Q*-point of the transistor, we begin by tabulating a few (V_{GS}, I_D) pairs.

V_{GS}	I_D
0 V	10 mA
−3.5 V	0 mA
$V_P/2 = -3.5/2 = -1.75$ V	$10 \times [1 - (-1.75)/(-3.5)]^2 = 2.5$ mA
$0.3V_P = 0.3 \times (-3.5) = -1.05$ V	$10 \times [1 - (-1.05)/(-3.5)]^2 = 4.9$ mA

Next, we turn to the voltage-divider bias line. Applying Kirchhoff's voltage law to the gate-source junction of the network,

$$V_G - V_{GS} - V_{R_S} = 0 \rightarrow V_{GS} = V_G - V_{R_S}$$

Here, the voltage V_{R_S} across the source resistance equals $I_S R_S$ or, equivalently, $I_D R_S$, giving

$$V_{GS} = V_G - I_D R_S$$

This equation plots as a straight line on the V_{GS}-I_D plane. Substituting $V_G = 2.16$ V and $R_S = 1.1$ kΩ brings to

$$V_{GS} = V_G - I_D R_S \rightarrow V_{GS} = 2.16 - 1.1 I_D$$

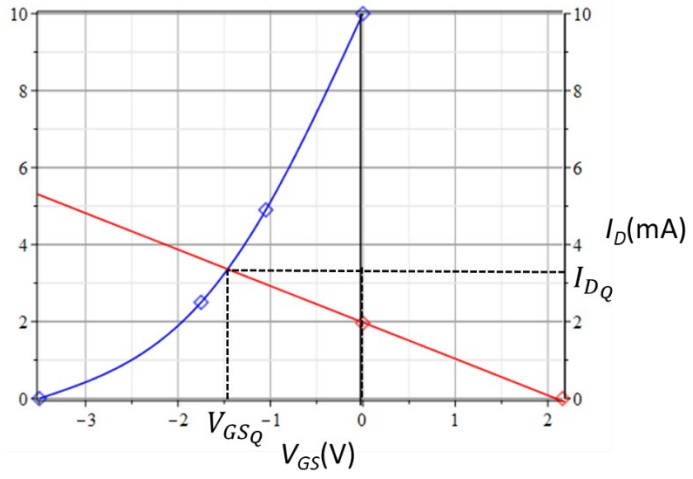
One point can be defined by setting V_{GS} to zero and solving for I_D,

$$0 = 2.16 - 1.1 I_D \rightarrow I_D = \frac{2.16}{1.1} = 1.96\,\text{mA}$$

Likewise, a second point can be defined by setting I_D to zero and solving for V_{GS},

$$V_{DS} = 2.16 - 1.1 \times 0 \rightarrow V_{GS} = 2.16\,\text{V}$$

Thus, the voltage-divider biasing line passes through (0, 1.96) and (2.16, 0), as shown. By inspection, we read $V_{GS_Q} \approx -1.5$ V and $I_{D_Q} \approx 3.3$ mA.



Now, the drain voltage is given by

$$V_D = V_{DD} - I_{D_Q} R_D = 20 - 3.3 \times 2.2 = \boxed{12.74\,\text{V}}$$

Noting that $I_S = I_D$, the source voltage is found as

$$V_S = I_S R_S = I_D R_S = 3.3 \times 1.1 = \boxed{3.63\,\text{V}}$$

The drain-source voltage under quiescent conditions is

$$V_{DS_Q} = V_{DD} - I_{D_Q}(R_D + R_S) = 20 - 3.3 \times (2.2 + 1.1) = \boxed{9.11\,\text{V}}$$

Problem 35.2: In this case, the transfer curve remains unchanged because the transistor is the same. The voltage-divider bias line, however, is now given by

$$V_{GS} = V_G - I_D R_S' \rightarrow V_{GS} = 2.16 - 0.51 I_D$$

As before, one point can be found by setting $V_{GS} = 0$ and solving for I_D,

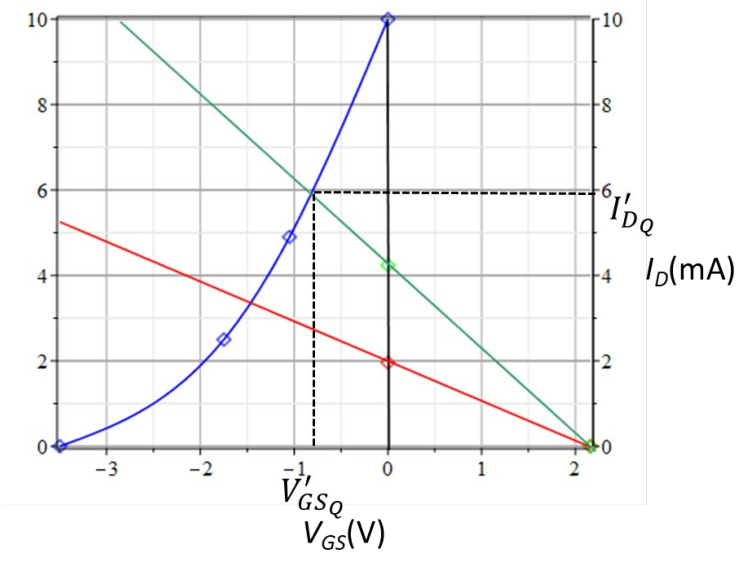
$$0 = 2.16 - 0.51 I_D \rightarrow I_D = \frac{2.16}{0.51} = 4.24\,\text{mA}$$

Setting I_D to zero and solving for V_{GS} yields

$$V_{DS} = 2.16 - 0.51 \times 0 \rightarrow V_{GS} = 2.16\,\text{V}$$

Thus, the updated voltage-divider bias line passes through (0, 4.24) and (2.16, 0), as shown in the green line below; the bias line for the higher

source resistance setting is redrawn for convenience. Inspecting the graph, we read the new intercepts $V'_{GS_Q} \approx -0.85$ V and $I'_{D_Q} \approx 5.9$ mA. Compare this with $V_{GS_Q} = -1.5$ V and $I_{D_Q} = 3.3$ mA and we see that halving the source resistance leads to a 43% decrease in the absolute value of V_{GS_Q} and a 79% increase in I_{D_Q}.



We proceed to compute the updated drain voltage V_D,

$$V_D = V_{DD} - I_{D_Q} R_D = 20 - 5.9 \times 2.2 = \boxed{7.02\,\text{V}}$$

the updated source voltage V_S,

$$V_S = I_D R_S = 5.9 \times 0.51 = \boxed{3.01\,\text{V}}$$

and the quiescent V_{DS},

$$V_{DS} = V_D - V_S = 7.02 - 3.01 = \boxed{4.01\,\text{V}}$$

P.36 ➡ Solution

Since we already have the drain-to-ground voltage V_D, there is no need to work with transfer curves.

$$V_{DD} - I_D R_D = V_D \rightarrow I_D = \frac{V_{DD} - V_D}{R_D}$$

$$\therefore I_D = \frac{18 - 12}{2} = \boxed{3\,\text{mA}}$$

The source voltage is

$$V_S = I_S R_S = I_D R_S = 3.0 \times 0.68 = \boxed{2.04\,\text{V}}$$

The drain-source voltage is

$$V_{DS} = V_{DD} - I_D \left(R_D + R_S \right) = 18 - 3.0 \times \left(2 + 0.68 \right) = \boxed{9.96\,\text{V}}$$

Using the voltage-divider rule, the gate voltage is calculated to be

$$V_G = \frac{110 \times 12}{110 + 680} = \boxed{1.67\ \text{V}}$$

The gate-source voltage easily follows,

$$V_{GS} = V_G - V_S = 1.67 - 2.04 = \boxed{-0.37\ \text{V}}$$

To find the pinch-off voltage, solve Shockley's equation for I_P, then substitute $V_{GS} = -0.37$ V, $I_{DSS} = 8$ mA, and $I_D = 3$ mA,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \rightarrow V_P = \frac{V_{GS}}{1 - \sqrt{\dfrac{I_D}{I_{DSS}}}}$$

$$\therefore V_P = \frac{-0.37}{1 - \sqrt{\dfrac{3.0}{8.0}}} = \boxed{-0.955\,\text{V}}$$

P.37 ➡ Solution

To establish the Q-point of the transistor, we first tabulate a few (V_{GS}, I_D) pairs.

V_{GS}	I_D
0 V	6 mA
−6 V	0 mA
$V_P/2 = -6/2 = -3$ V	$6 \times [1 - (-3)/(-6)]^2 = 1.5$ mA
$0.3V_P = 0.3 \times (-6) = -1.8$ V	$6 \times [1 - (-1.8)/(-6)]^2 = 2.94$mA

Next, we turn to the common-gate line. Applying Kirchhoff's voltage law to the gate-source junction of the network brings to

$$-V_{GS} - I_S R_S + V_{SS} = 0 \rightarrow V_{GS} = V_{SS} - I_S R_S$$

But, with $I_S = I_D$,

$$V_{GS} = V_{SS} - I_D R_S$$

The equation above defines the load line for a common-gate configuration. In the present case, $V_{SS} = 4$ V and $R_S = 2.2$ kΩ, so that

$$V_{GS} = 4 - 2.2 I_D$$

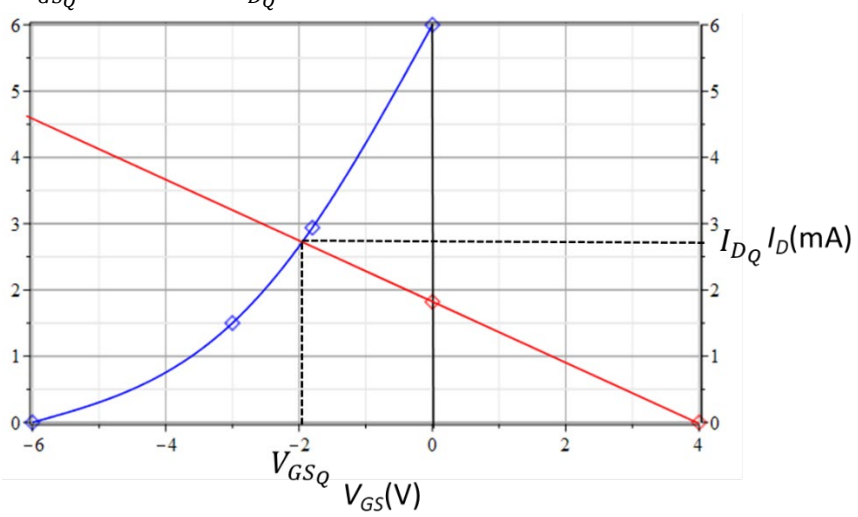
As always, two points are used to plot the line. First, setting V_{GS} to zero and solving for I_D,

$$0 = 4 - 2.2 I_D \rightarrow I_D = \frac{4}{2.2} = 1.82\,\text{mA}$$

That is, (0, 1.82) is the y-intercept of the load line. Next, setting I_D to zero and solving for V_{GS},

$$V_{GS} = 4 - 2.2 \times 0 = 4\,\text{V}$$

Accordingly, (4, 0) is the x-intercept of the line in question. We proceed to plot the transfer curve and the load line. The Q-point values are read as $V_{GS_Q} \approx -2$ V and $I_{D_Q} \approx 2.7$ mA.



We are now in position to determine the drain-source voltage V_{DS},

$$V_{DS} = V_{DD} + V_{SS} - I_D (R_D + R_S) = 16 + 4 - 2.7 \times (2.2 + 2.2) = \boxed{8.12\,\text{V}}$$

The source voltage V_S is

$$V_S = -V_{SS} + I_D R_S = -4 + 2.7 \times 2.2 = \boxed{1.94\,\text{V}}$$

Notice that $V_S \approx |V_{GS_Q}|$ because $V_G = 0$ V.

P.38 ➡ Solution

Since we already have the drain-source voltage $V_{DS} = 4$ V, we can establish drain current I_D without recourse to transfer curve analysis. Indeed,

$$V_{DS} = V_{DD} + V_{SS} - I_D (R_D + R_S) \rightarrow I_D = \frac{V_{DD} + V_{SS} - V_{DS}}{R_D + R_S}$$

$$\therefore I_D = \frac{20 - 2 - 4}{3.0 + 1.2} = \boxed{3.33\,\text{mA}}$$

The drain voltage V_D is

$$V_D = V_{DD} - I_D R_D = 20 - 3.33 \times 3 = \boxed{10\,\text{V}}$$

The source voltage V_S is, in turn,

$$V_S = -V_{SS} + I_D R_S = 2 + 3.33 \times 1.2 = \boxed{6.0\,\text{V}}$$

With $V_G = 0$ V, we obviously have

$$V_{GS} = V_G - V_S = 0 - 6.0 = \boxed{-6.0\,\text{V}}$$

P.39 ➡ *Solution*

Notice that the gate branch of the FET is organized in a voltage-divider bias topology. Using the voltage-divider rule, we find that

$$V_G = \frac{18\times 20}{91+18} = \boxed{3.30\ \text{V}}$$

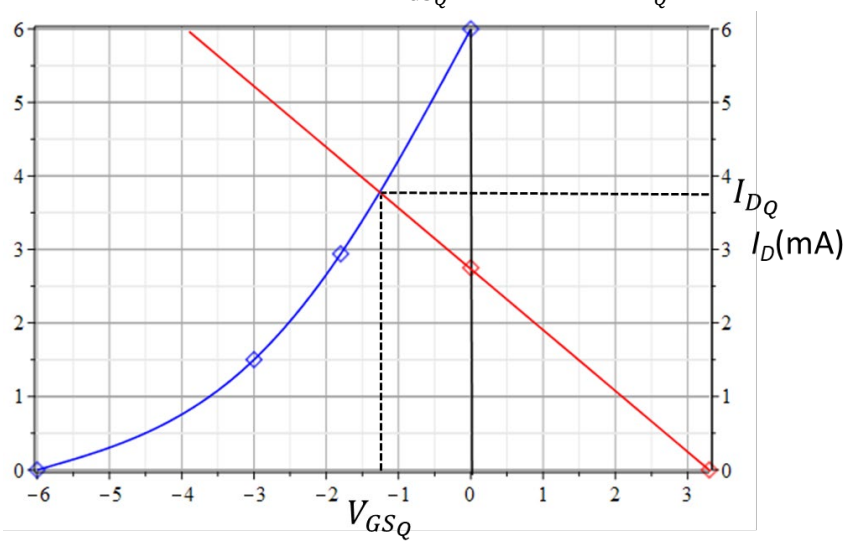
To find the Q-point variables, we need to perform a transfer curve-load line analysis. Some (V_{GS}, I_D) pairs are computed below.

V_{GS}	I_D
0 V	6 mA
−6 V	0 mA
$V_P/2 = -6/2 = -3$ V	$6 \times [1 - (-3)/(-6)]^2 = 1.5$ mA
$0.3V_P = 0.3 \times (-6) = -1.8$ V	$6 \times [1 - (-1.8)/(-6)]^2 = 2.94$mA

Further, since this is a voltage-divider bias configuration, the load line has the form

$$V_{GS} = V_G - I_D R_S \rightarrow V_{GS} = 3.30 - 1.2 I_D$$

and includes points (0, 2.75) and (3.30, 0). The graphs are shown below. The transfer curve and load line cross at $V_{GS_Q} \approx -1.2$ V and $I_{D_Q} \approx 3.8$ mA.



Notice that the drain branch of the FET is connected to the emitter branch of the BJT; therefore, we can state that

$$I_E = I_{D_Q} = \boxed{3.8\,\text{mA}}$$

The base current can be found with the value of I_E and the current gain parameter $\beta = 160$:

$$I_B = \frac{I_E}{1+\beta} = \frac{3.8}{1+160} = 0.0238\,\text{mA} = \boxed{23.8\,\mu\text{A}}$$

In the present topology, the drain voltage V_D is equivalent to the emitter voltage V_E,

$$V_D = V_E = V_B - V_{BE} = (V_{CC} - I_B R_B) - V_{BE}$$

$$\therefore V_D = 20 - 0.0238\times 330 - 0.7 = \boxed{11.45\,\text{V}}$$

The collector voltage V_C is

$$V_C = V_{CC} - \underbrace{I_C}_{\approx I_E} R_C = 20 - 3.8\times 1.1 = \boxed{15.82\,\text{V}}$$

P.40 ➡ *Solution*

The base voltage V_B of the BJT is equivalent to the gate voltage V_G of the FET, and can be determined with the voltage-divider rule:

$$V_B = V_G = \frac{10\times 16}{40+10} = \boxed{3.2\,\text{V}}$$

(Recall that for a BJT voltage-divider bias topology, this approximation requires that $\beta R_E \geq 10R_2$, which can be shown to be true in this situation.) Noting that $V_{BE} = 0.7$ V, the emitter voltage follows as

$$V_{BE} = V_B - V_E \rightarrow V_E = V_B - V_{BE}$$

$$\therefore V_E = 3.2 - 0.7 = \boxed{2.5\,\text{V}}$$

Applying Ohm's law to the emitter branch of the BJT, we get

$$V_E = I_E R_E \rightarrow I_E = \frac{V_E}{R_E}$$

$$\therefore I_E = \frac{2.5}{1.2} = \boxed{2.08\,\text{mA}}$$

With I_E = 2.08 mA and β = 100, the collector current is determined as

$$I_C = \left(\frac{\beta}{1+\beta}\right) I_E = \left(\frac{100}{1+100}\right) \times 2.08 = \boxed{2.06\,\text{mA}}$$

The collector current of the BJT functions as source current for the FET; that is,

$$I_C = I_S = 2.06\,\text{mA}$$

Further,

$$I_D = I_S = \boxed{2.06\,\text{mA}}$$

With β = 100 and I_C = 2.06 mA, we write

$$I_B = \frac{I_C}{\beta} = \frac{2.06}{100} = 0.0206\,\text{mA} = \boxed{20.6\,\mu\text{A}}$$

To find collector voltage V_C, first note that $V_C = V_S$. Accordingly, we write

$$V_{GS} = V_G - V_S \rightarrow V_C = V_G - V_{GS}$$

Here, V_G = 3.2 V and V_{GS} can be determined with Shockley's equation,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \rightarrow V_{GS} = V_P \times \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$\therefore V_{GS} = -6 \times \left(1 - \sqrt{\frac{2.06}{6.0}}\right) = -2.48\,\text{V}$$

so that

$$V_C = 3.2 - (-2.48) = \boxed{5.68\,\text{V}}$$

Further,

$$V_S = V_C = \boxed{5.68\,\text{V}}$$

Applying KVL to the drain branch of the FET should yield voltage V_D

$$V_D = V_{DD} - I_D R_D = 16 - 2.06 \times 2.2 = \boxed{11.47\,\text{V}}$$

With V_C = 5.68 V and V_E = 2.5 V, the collector-emitter voltage is determined as

$$V_{CE} = V_C - V_E = 5.68 - 2.5 = \boxed{3.18\,\text{V}}$$

With V_D = 11.47 V and V_S = 5.68 V, the drain-source voltage is calculated as

$$V_{DS} = V_D - V_S = 11.47 - 5.68 = \boxed{5.79\,\text{V}}$$

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