# Quiz EL303
# CMOS Logic Gates

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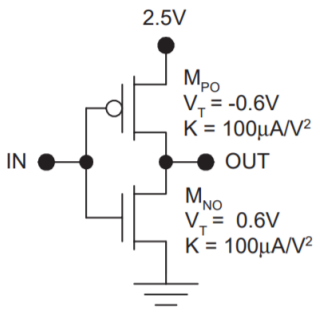
## PROBLEM DISTRIBUTION

| Problems | Subject |
|---|---|
| 1 – 3 | Basic CMOS inverter modelling |
| 4 – 5 | CMOS inverter circuits |
| 5 – 13 | CMOS logic gates |
| 14 – 16 | Power dissipation |

## PROBLEMS

### Problem 1 (Modified from Ayers, 2004)

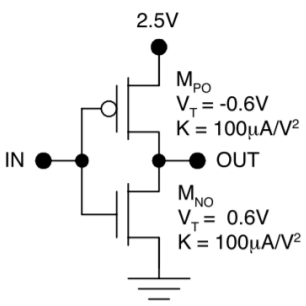
Plot the voltage transfer characteristic for the symmetric CMOS inverter illustrated to the side if supply voltage $V_{DD}$ = 2.5 V, threshold voltage $V_T$ = 0.6 V, and transconductance parameter $K$ = 100 μA/V².




*Hint:* Refer to Table 1 in the Additional Information section.

### Problem 2 (Modified from Ayers, 2004)

Plot the short-circuit current *vs.* input voltage curve for the symmetric CMOS inverter illustrated to the side if supply voltage $V_{DD}$ = 2.5 V, threshold voltage $V_T$ = 0.6 V, and transconductance parameter $K$ = 100 μA/V².



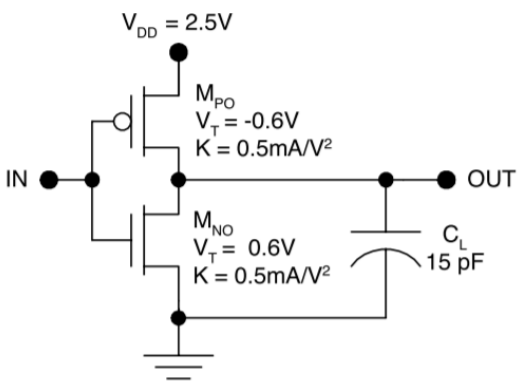

*Hint:* Refer to Table 2 in the Additional Information section.

### Problem 3 (Modified from Ayers, 2004)

Estimate the propagation delay $t_p$ for the symmetric CMOS inverter illustrated below if supply voltage $V_{DD}$ = 2.5 V, threshold voltage $V_T$ = 0.6 V, and transconductance parameter $K$ = 0.5 mA/V². The load is $C_L$ = 18 pF.

*Hint:* Recall that $t_p$ can be estimated as

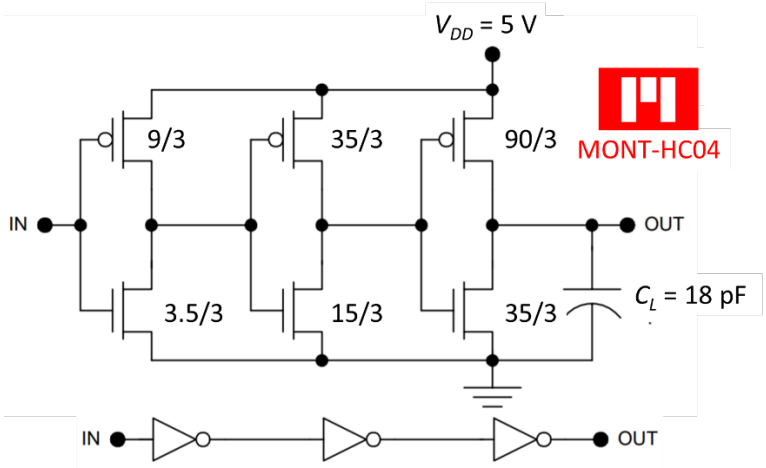
$$t_p = \frac{C_L}{K}\left[\frac{2V_T}{(V_{DD}-V_T)^2} + \frac{2}{(V_{DD}-V_T)}\ln\left(\frac{V_{DD}-V_T}{V_{DD}/2}\right)\right]$$



## Problem 4 (Modified from Ayers, 2004)

Estimate the propagation delay for the MONT-HC04 three-stage CMOS illustrated below with a 18-pF load. The specifications of the CMOS technology at hand are given in the following table. Use $\mu_n$ = 230 cm$^2$/V·s and $\mu_p$ = 580 cm$^2$/V·s as the values of electron and hole mobility, respectively. The numbers next to each transistor are the width (numerator) and length (denominator) of each device.

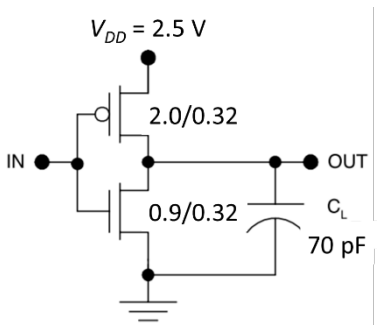
| Gate material | Polysilicon |
|---|---|
| Gate length | 3 µm |
| Oxide thickness | 60 nm |
| Supply voltage | 5.0 V |



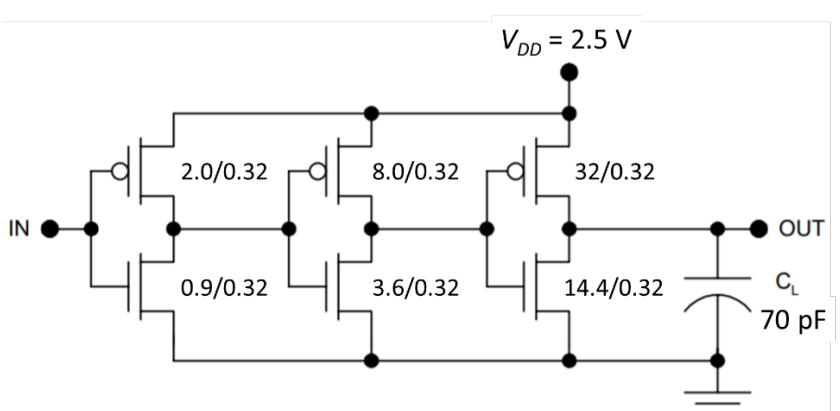

■ A modern VLSI CMOS chip contains a million or more gates but only ~$10^3$ external connections. Therefore, most of the gates experience only on-chip loads and are capable of propagation delays in picoseconds without the need for buffering. For the externally connected gates, significant capacitive loading exists, so buffering is necessary to reduce propagation delays and achieve acceptable off-chip data rates. Problem 5 illustrates use of buffer stages in a CMOS circuit. In 5.1, we analyze a simple inverter with no buffering stages; then, in 5.2 we investigate a CMOS circuit with two stages of buffering.

## Problem 5 (Modified from Ayers, 2004)

**Problem 5.1:** Estimate the propagation delay for a single CMOS driving a 70-pF off-chip load as illustrated below. Assume 0.32-micron CMOS technology using a 2.5-V supply for all gates, including the output drivers, and ±0.5-V threshold voltages. For this technology, the inverters internal to the chip have gate dimensions of 2.0 µm/0.32 µm (*p*-MOSFET) and 0.9 µm/0.32 µm (*n*-MOSFET) and the oxide thickness is 6 nm. Use $\mu_n$ = 230 cm$^2$/V·s and $\mu_p$ = 580 cm$^2$/V·s as the values of electron and hole mobility, respectively.

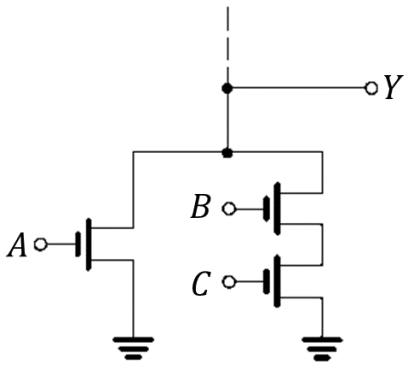



**Problem 5.2:** Estimate the propagation delay for three stages of CMOS driving a 70-pF off-chip load if a scaling factor of four is applied to each stage of buffering. Other data remain as specified in the previous problem.

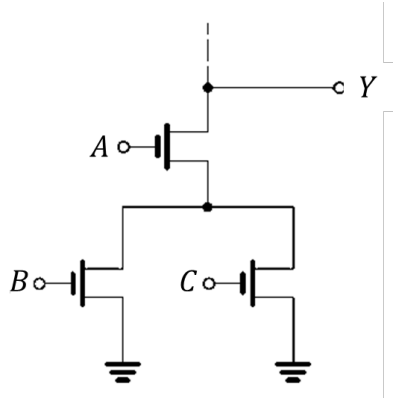


## Problem 6 (Sedra and Smith, 2015)

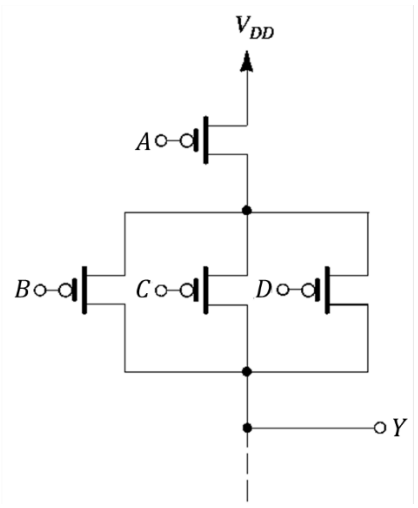
**Problem 6.1:** Find the pull-up network that corresponds to the pull-down network illustrated below, and hence the complete CMOS logic circuit. What is the Boolean function realized?




**Problem 6.2:** Find the pull-up network that corresponds to the pull-down network illustrated below, and hence the complete CMOS logic circuit. What is the Boolean function realized?




**Problem 6.3:** Find the pull-down network that corresponds to the pull-up network illustrated below. What is the Boolean function realized?




## Problem 7 (Sedra and Smith, 2015)

**Problem 7.1:** Give the CMOS realization for the Boolean function

$$Y = \overline{(A+B)(C+D)}$$

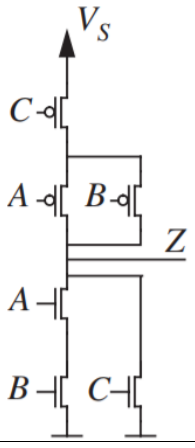
**Problem 7.2:** Sketch a CMOS logic circuit that realizes the function $Y = AB + \bar{A}\bar{B}$. This is called the **equivalence** or **coincidence function**.

**Problem 7.3:** Sketch a CMOS logic circuit that realizes the function $Y = ABC + \bar{A}\bar{B}\bar{C}$.

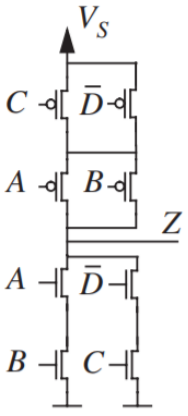
## Problem 8 (Agarwal and Lang, 2005)

Write a truth table and a Boolean expression that describes the operation of each of the digital circuits illustrated below.

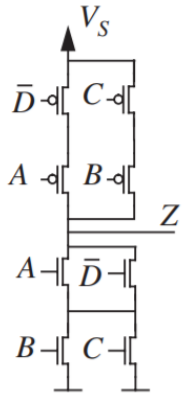
**Problem 8.1**



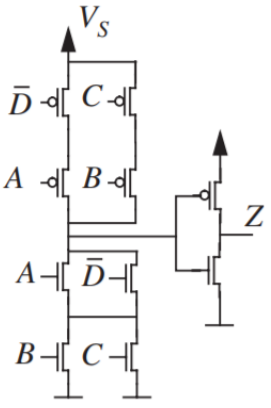

**Problem 8.2**




**Problem 8.3**




**Problem 8.4**




## Problem 9 (Rabaey *et al.*, 2003)

Implement the equation $X = ((\bar{A} + \bar{B})(\bar{\bar{C}} + \bar{D} + \bar{E}) + \bar{F})\bar{G}$ using complementary CMOS. Size the devices so that the output resistance is the same as that of an inverter with an NMOS width-to-length ratio $W/L = 2$ and PMOS width-to-length ratio $W/L = 6$. Which input pattern(s) would give the best and worst equivalent pull-up or pull-down resistance?

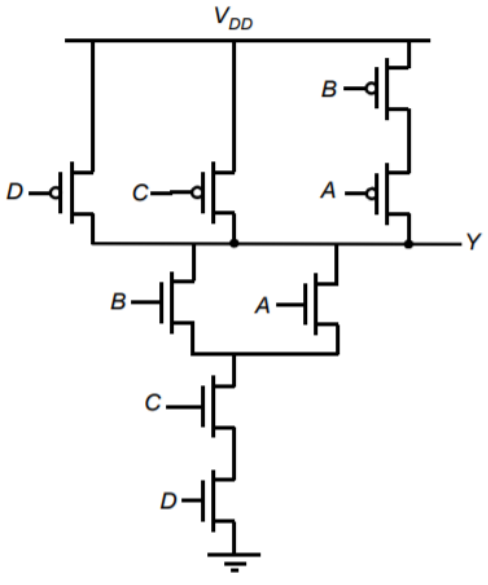
## Problem 10 (Rabaey *et al.*, 2003)

Implement the following expression in a full static CMOS logic fashion using no more than 10 transistors.

$$Y = AB + ACE + DE + DCB$$

## Problem 11 (Rabaey *et al.*, 2003)

Consider the circuit illustrated below. Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS width-to-length ratio $W/L = 4$ and a PMOS $W/L = 8$.



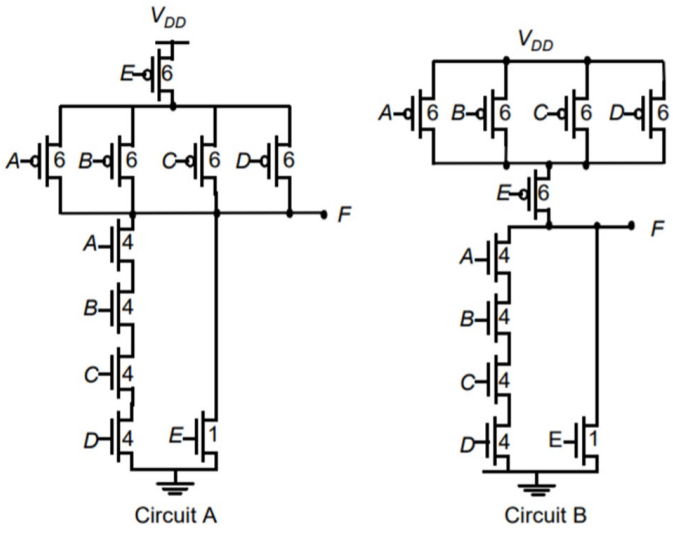
## Problem 12 (Rabaey *et al.*, 2003)

Consider the following CMOS circuits.

**Problem 12.1:** Do the following circuits implement the same logic function? If yes, what is that logic function? If no, give Boolean expressions for both circuits.

**Problem 12.2:** Will these two circuits' output resistances always be equal to each other?

**Problem 12.3:** Will these two circuits' rise and fall times always be equal to each other? Why or why not?



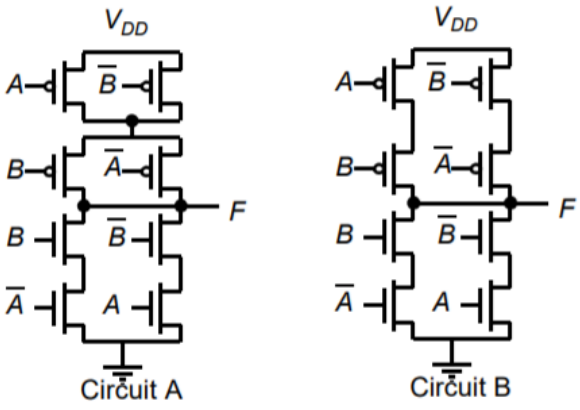

**Problem 12.4:** Reconsider circuits *A* and *B* illustrated above. The transistors in the circuits have been sized to give an output resistance of 13 kΩ for the worst-case input pattern. This output resistance can vary, however, if other patterns are applied.

→ What input patterns (*A* – *E*) give the lowest output resistance when the output is low? What is the value of that resistance?

→ What input patterns (*A* – *E*) give the lowest output resistance when the output is high? What is the value of that resistance?

## Problem 13 (Rabaey *et al.*, 2003)

What is the logic function of circuits *A* and *B* in the figure below? Which one is a dual network and which one is not? Is the nondual network still a valid logic gate? Explain. List any advantages of one configuration over the other.




■ The power loss of an IC to charge or discharge load capacitance is modeled as

$$P_{IC} = \frac{1}{2}\alpha C_L V_{DD}^2 f_{clk}$$

where $P_{IC}$ is the power dissipated on the active edge of the clock when load capacitance is charged or discharged, $\alpha$ is the average IC switching activity coefficient, $C_L$ is a lump sum capacitance for all signal switching nodes in the IC, and $f_{clk}$ is the clock frequency. During each clock pulse, only a fraction $\alpha$ of the combinational logic gates undergo a transition, and the load capacitance is either charged or discharged but not both. $\alpha$ is typically on the order of 5 – 30% for combinational logic gates in various ICs.

Note that the power required to charge and discharge a logic gate capacitance in a *clock network* is

$$P_{IC} = \alpha C_L V_{DD}^2 f_{clk}$$

where $\alpha = 1$ since the clock pulse is deterministic and happens with certainty on each period. The 1/2 factor that distinguishes the two previous equations disappears in the latter because charge and discharge are involved in the same

clock period. Some clock networks gate the clock for subcircuits that are not activated during an operation. This allows de-powering of that subcircuit.
In Problems 14 to 16, we use $\alpha$ at the gate level to compare the power efficiency of different logic gates to better understand power reduction. Products may be high-performance high-power or low-frequency low-power ICs, but all products must minimize power dissipation.
Assume that the major power dissipation occurs when the clock makes an active transition. The probability of an output signal transition from zero to one is $\alpha_{0\to1}$ and may be expressed as

$$\alpha_{0\to1} = p_0 p_1 = p_0\left(1-p_0\right)$$

where $p_0$ is the probability of an output logic-0 and $p_1$ is the probability of an input logic-1. The probability of an output signal transition from 1 to 0 is $\alpha_{1\to0}$ and may be represented as

$$\alpha_{1\to0} = p_1 p_0 = p_1\left(1-p_1\right)$$

so that

$$\alpha_{0\to1} = \alpha_{1\to0}$$

Quantities $\alpha_{0\to1}$ and $\alpha_{1\to0}$ are known as *transition* or *switching activity coefficients*. If the input logic states are random, then we can determine $p_0$ and $p_1$, and thence the activity coefficients. Let $N_0$ denote the number of possible logic-0 states in the output of a logic state, $N_1$ the number of possible logic-1 states in the output of a logic state, and $N$ the number of input signals feeding the logic circuit. The total number of input logic states is $2^N$. It follows that

$$p_0 = \frac{N_0}{2^N} \;\; ; \;\; p_1 = \frac{N_1}{2^N}$$

The transition activity coefficient is then restated as

$$\alpha_{0\to1} = p_0 p_1 = \frac{N_0}{2^N}\times\frac{N_1}{2^N} = \frac{N_0 N_1}{2^{2N}} = \frac{N_0\left(2^N - N_0\right)}{2^{2N}}$$

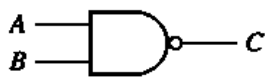
where we have used the relation $N_0 + N_1 = 2^N$.
We treat the inputs to combinational logic as random. A random input to an inverter considers that two consecutive zeros and ones could occur that would not cause a logic transition. If the inputs to an inverter are random then the probability of a 0 → 1 or a 1 → 0 transition is

$$\alpha_{\text{Inv}} = \alpha_{0\to1} + \alpha_{1\to0} = p_0 p_1 + p_1 p_0 = \frac{1}{2}\times\frac{1}{2} + \frac{1}{2}\times\frac{1}{2} = 0.5$$

The inverter has a 0.5 probability of changing state when admitting a random input – an intuitively obvious result.

## Problem 14 (Hawkins *et al.*, 2013)

**Problem 14.1:** Calculate the activity coefficient $\alpha_{0\to1}$ for a 2NAND gate using a truth table to identify the number of states.




**Problem 14.2:** If the NAND gate is clocked at 1 GHz, fed by a power supply of 1.5 V, and a load of 200 fF, what is the expected power dissipation of that gate for the 0 → 1 transition?

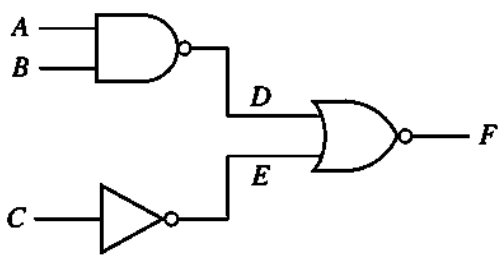
**Problem 14.3:** If an IC has one million such gates, each with an activity coefficient of 20%, what is the operating power of the IC due to the combinational logic gates?

## Problem 15 (Hawkins *et al.*, 2013)

**Problem 15.1:** In the following logic network, load capacitance $C_L$ = 50 fF, supply voltage $V_{DD}$ = 2.0 V, and clock frequency $f_{clk}$ = 1.5 GHz. Make a truth table for the circuit and calculate the switching activity coefficient $\alpha_{0\to1}$ including the activity coefficients for all gate output nodes.

*Hint:* You must calculate and add the transition probabilities for each of the signal nodes *D*, *E*, and *F*.

**Problem 15.2:** Calculate the expected power dissipation in the 0 → 1 transition.



## Problem 16 (Hawkins *et al.*, 2013)

Given the logic operation $F = A(B + CD)$, supply voltage $V_{DD}$ = 1.2 V, load capacitance $C_L$ = 115 fF, and clock frequency $f_{clk}$ = 1.6 GHz:

**Problem 16.1:** Draw the transistor schematic for a static CMOS gate that implements logic function $F$.

**Problem 16.2:** Compute the activity coefficients for both output transitions using a truth table.

**Problem 16.3:** Calculate the expected power dissipated.

## ADDITIONAL INFORMATION

**Table 1** Voltage transfer characteristic intervals for a symmetric CMOS inverter*

| | Range of $V_{IN}$ | $p$-MOS mode | $n$-MOS mode | Equation for output voltage $V_{OUT}$ |
|---|---|---|---|---|
| 1 | $V_{IN} \le V_T$ | Linear | Cutoff | $V_{OUT} = V_{DD}$ |
| 2 | $V_T \le V_{IN} \le V_{OUT} - V_T$ | Linear | Saturation | $V_{OUT} = (V_{IN} + V_T) + \sqrt{(V_{IN} - V_{DD} + V_T)^2 - (V_{IN} - V_T)^2}$ |
| 3 | $V_{OUT} - V_T \le V_{IN} \le V_{OUT} + V_T$ | Saturation | Saturation | Interpolate |
| 4 | $V_{OUT} + V_T \le V_{IN} \le V_{OUT} - V_T$ | Saturation | Linear | $V_{OUT} = (V_{IN} - V_T) + \sqrt{(V_{IN} - V_T)^2 - (V_{IN} - V_{DD} + V_T)^2}$ |
| 5 | $V_{IN} \ge V_{DD} - V_T$ | Cutoff | Linear | $V_{OUT} = 0$ |

*Transconductances $K_N$ and $K_P$ are equal and lumped together in a parameter $K$. Likewise, threshold voltages are such that $V_{TN} = |V_{TP}| = V_T$. $V_{DD}$ denotes supply voltage.

**Table 2** Short-circuit current in a symmetric CMOS inverter*

| | Range of $V_{IN}$ | Operation description | *Equation for short-circuit current $I_{DD}$* |
|---|---|---|---|
| 1 | $V_{IN} \le V_T$ | $n$-MOSFET is cut off and no current flows | $I_{DD} = 0$ |
| 2 | $V_T \le V_{IN} \le V_{DD}/2$ | $n$-MOSFET is saturated | $I_{DD} = \frac{K(V_{IN} - V_T)^2}{2}$ |
| 3 | $V_{DD}/2 \le V_{IN} \le V_{DD} - V_T$ | $p$-MOSFET is saturated | $I_{DD} = \frac{K(V_{IN} - V_{DD} + V_T)^2}{2}$ |
| 4 | $V_{IN} \ge V_{DD} - V_T$ | $p$-MOSFET is cut off and no current flows | $I_{DD} = 0$ |

*$K$ and $V_T$ follow the same simplifications used in Table 1.

## SOLUTIONS

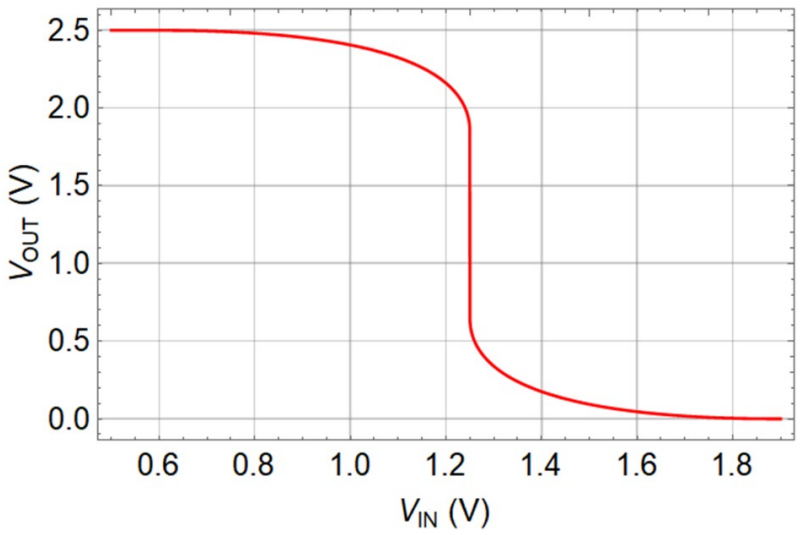
### P.1 ➡ *Solution*

Refer to Table 1 in the Additional Information section. The voltage transfer characteristic can be divided piecewise in 5 parts, each of which are computed below,

$$V_{OUT} = \begin{cases} V_{DD}, \text{if } V_{IN} \le 0.6\,\text{V} \\ (V_{IN} + 0.6) + \sqrt{(V_{IN} - 2.5 + 0.6)^2 - (V_{IN} - 0.6)^2}, \text{if } 0.6 \le V_{IN} \le 1.25\,\text{V} \\ 1.25\,\text{V}, \text{ if } V_{IN} = 1.25\,\text{V} \\ (V_{IN} - 0.6) - \sqrt{(V_{IN} - 0.6)^2 - (V_{IN} - 2.5 + 0.6)^2}, \text{ if } 1.25\,\text{V} \le V_{IN} \le 1.9\,\text{V} \\ 0, \text{if } V_{IN} \ge 1.9\,\text{V} \end{cases}$$

$$\therefore V_{OUT} = \begin{cases} 2.5, \text{if } V_{IN} \le 0.6\,\text{V} \\ (V_{IN} + 0.6) + \sqrt{(V_{IN} - 1.9)^2 - (V_{IN} - 0.6)^2}, \text{if } 0.6 \le V_{IN} \le 1.25\,\text{V} \\ 1.25\,\text{V}, \text{ if } V_{IN} = 1.25\,\text{V} \\ (V_{IN} - 0.6) - \sqrt{(V_{IN} - 0.6)^2 - (V_{IN} - 1.9)^2}, \text{ if } 1.25\,\text{V} \le V_{IN} \le 1.9\,\text{V} \\ 0, \text{if } V_{IN} \ge 1.9\,\text{V} \end{cases}$$

For this example, both transistors are saturated only at $V_{IN} = V_{DD}/2$, so no interpolation is needed. The characteristic is plotted below. For a symmetric CMOS inverter with matched transistors, the characteristic exhibits odd symmetry about the vertical line $V_{IN} = V_{DD}/2 = 1.25$.



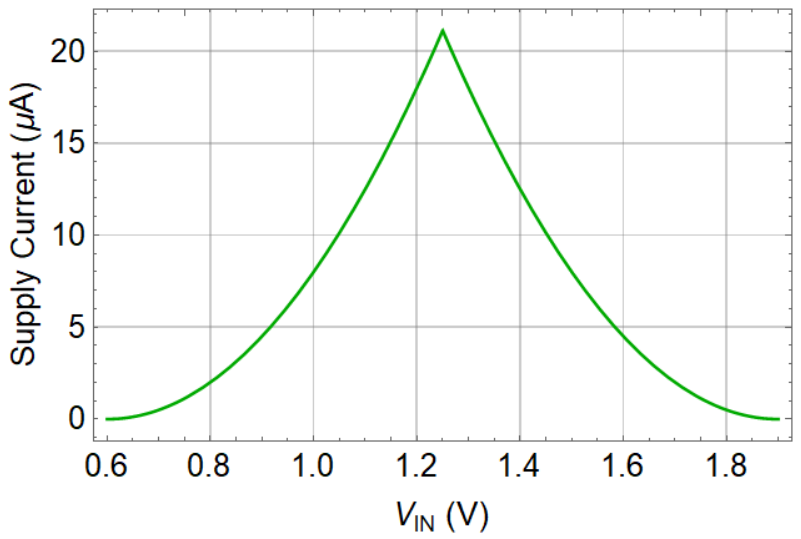

## P.2 ➡ *Solution*

Refer to Table 2 in the Additional Information section. The short-circuit current curve can be divided piecewise in 4 parts, each of which are computed below,

$$I_{DD} = \begin{cases} 0, \text{if } V_{IN} \le 0.6\,\text{V} \\ \dfrac{100\times\left(V_{IN}-0.6\right)^2}{2}, \text{if } 0.6 \le V_{IN} \le 2.5/2 \\ \dfrac{100\times\left(V_{IN}-2.5+0.6\right)^2}{2}, \text{if } 2.5/2 \le V_{IN} \le 2.5-0.6 \\ 0, \text{ if } V_{IN} \ge 2.5-0.6 \end{cases}$$

$$\therefore I_{DD} = \begin{cases} 0, \text{if } V_{IN} \le 0.6\,\text{V} \\ 50\left(V_{IN}-0.6\right)^2, \text{if } 0.6 \le V_{IN} \le 1.25 \\ 50\left(V_{IN}-1.9\right)^2, \text{if } 1.25 \le V_{IN} \le 1.9 \\ 0, \text{ if } V_{IN} \ge 1.9 \end{cases}$$

These expressions are plotted below. Note that the vertical axis displays currents in μA. As can be seen, the short-circuit current is maximum when the input voltage equals half the supply voltage.




## P.3 ➡ *Solution*

Simply substitute the data into the formula for $t_p$,

$$t_p = \frac{18\times10^{-15}}{0.5\times10^{-3}}\left[\frac{2\times0.6}{\left(2.5-0.6\right)^2}+\frac{2}{\left(2.5-0.6\right)}\ln\left(\frac{2.5-0.6}{2.5/2}\right)\right] = \boxed{27.8\,\text{ns}}$$

Note that the formula in question indicates that delay times are directly proportional to load capacitance and inversely proportional to device transconductance and (to an approximate extent) supply voltage. These relationships have led some designers to use the crude approximation

$$t_p \approx \frac{2C_L}{KV_{DD}}$$

In the present case,

$$t_p \approx \frac{2\times\left(18\times10^{-12}\right)}{\left(0.5\times10^{-3}\right)\times2.5} = 28.8\,\text{ns}$$

The approximation above overestimates the delay time by 3.6%, which is a reasonably accurate result.

## P.4 ➡ *Solution*

We begin by computing the process transconductance parameters for the *p*-MOSFETs and *n*-MOSFETs, namely

$$k_p' = \frac{\mu_p\varepsilon_{ox}}{t_{ox}} = \frac{230\times\left[3.9\times\left(8.85\times10^{-14}\right)\right]}{60\times10^{-7}} = 13.2\,\mu\text{A/V}^2$$

$$k_n' = \frac{\mu_n\varepsilon_{ox}}{t_{ox}} = \frac{580\times\left[3.9\times\left(8.85\times10^{-14}\right)\right]}{60\times10^{-7}} = 33.4\,\mu\text{A/V}^2$$

For the first stage, the device transconductance parameters are

$$K_{p,1} = k_p'\frac{W_{p1}}{L_{p1}} = 13.2\times\left(\frac{9}{3}\right) = 39.6\,\mu\text{A/V}^2$$

$$K_{N,1} = k_N'\frac{W_{N1}}{L_{N1}} = 33.4\times\left(\frac{3.5}{3}\right) = 39.0\,\mu\text{A/V}^2$$

Now, the load capacitance seen by the first stage is the input capacitance for the second stage, namely

$$C_{L,1} = \frac{\varepsilon_{ox}W_{P2}L_{P2}}{t_{ox}} + \frac{\varepsilon_{ox}W_{N2}L_{N2}}{t_{ox}}$$

$$\therefore C_{L,1} = \frac{\left[3.9\times\left(8.85\times10^{-14}\right)\right]\times\left(35\times10^{-6}\right)\times\left(3\times10^{-6}\right)}{60\times10^{-9}} + \frac{\left[3.9\times\left(8.85\times10^{-14}\right)\right]\times\left(15\times10^{-6}\right)\times\left(3\times10^{-6}\right)}{60\times10^{-9}} = 86.3\,\text{fF}$$

The propagation delay is computed with the formula introduced in Problem 3,

$$t_p = \frac{C_L}{K}\left[\frac{2V_T}{\left(V_{DD}-V_T\right)^2} + \frac{2}{\left(V_{DD}-V_T\right)}\ln\left(\frac{V_{DD}-V_T}{V_{DD}/2}\right)\right]$$

$$\therefore t_{p,1} = \frac{86.3\times10^{-15}}{39.6\times10^{-6}}\left[\frac{2\times0.6}{\left(5.0-0.6\right)^2} + \frac{2}{\left(5.0-0.6\right)}\ln\left(\frac{5.0-0.6}{5.0/2}\right)\right] = 0.7\,\text{ns}$$

Moving on to the second stage, the device transconductance parameters are

$$K_{p,2} = k_p'\frac{W_{p2}}{L_{p2}} = 13.2\times\left(\frac{35}{3}\right) = 154\,\mu\text{A/V}^2 = 0.154\,\text{mA/V}^2$$

$$K_{N,2} = k_N'\frac{W_{N2}}{L_{N2}} = 33.4\times\left(\frac{15}{3}\right) = 167\,\mu\text{A/V}^2 = 0.167\,\text{mA/V}^2$$

The load capacitance seen by the second stage is the input capacitance for the third stage,

$$C_{L,2} = \frac{\varepsilon_{ox}W_{P3}L_{P3}}{t_{ox}} + \frac{\varepsilon_{ox}W_{N3}L_{N3}}{t_{ox}}$$

$$\therefore C_{L,2} = \frac{\left[3.9\times\left(8.85\times10^{-14}\right)\right]\times\left(90\times10^{-6}\right)\times\left(3\times10^{-6}\right)}{60\times10^{-9}} + \frac{\left[3.9\times\left(8.85\times10^{-14}\right)\right]\times\left(35\times10^{-6}\right)\times\left(3\times10^{-6}\right)}{60\times10^{-9}} = 216\,\text{fF}$$

The propagation delay follows as

$$t_{p,2} = \frac{216\times10^{-15}}{0.154\times10^{-3}}\left[\frac{2\times0.6}{(5.0-0.6)^2}+\frac{2}{(5.0-0.6)}\ln\left(\frac{5.0-0.6}{5.0/2}\right)\right] = 0.447\,\text{ns}$$

For the third stage, the device transconductance parameters are

$$K_{p,3} = k'_p\frac{W_{p3}}{L_{p3}} = 13.2\times\left(\frac{90}{3}\right) = 396\,\mu\text{A/V}^2 = 0.396\,\text{mA/V}^2$$

$$K_{N,3} = k'_N\frac{W_{N3}}{L_{N3}} = 33.4\times\left(\frac{35}{3}\right) = 390\,\mu\text{A/V}^2 = 0.390\,\text{mA/V}^2$$

The load capacitance seen by the third stage is the external load $C_{L3}$ = 18 pF, and the propagation delay for the third stage is

$$t_{p,3} = \frac{18\times10^{-12}}{0.396\times10^{-3}}\left[\frac{2\times0.6}{(5.0-0.6)^2}+\frac{2}{(5.0-0.6)}\ln\left(\frac{5.0-0.6}{5.0/2}\right)\right] = 14.5\,\text{ns}$$

The overall propagation delay for the MONT-HC04 inverter with a 18-pF external load can be found by adding the individual propagation delays of the three stages:

$$t_p = t_{p,1}+t_{p,2}+t_{p,3} = 0.7+0.447+14.5 = \boxed{15.6\,\text{ns}}$$

## P.5 ➡ *Solution*

**Problem 5.1:** The first step is to compute the process technology parameters $k'_p$ and $k'_N$,

$$k'_p = \frac{\mu_p\varepsilon_{ox}}{t_{ox}} = \frac{230\times\left[3.9\times\left(8.85\times10^{-14}\right)\right]}{6.0\times10^{-7}} = 0.132\,\text{mA/V}^2$$

$$k'_n = \frac{\mu_n\varepsilon_{ox}}{t_{ox}} = \frac{580\times\left[3.9\times\left(8.85\times10^{-14}\right)\right]}{6.0\times10^{-7}} = 0.334\,\text{mA/V}^2$$

A single unbuffered stage drives an external 70-pF load. The corresponding transconductance parameters are

$$K_p = k'_p\frac{W_p}{L_p} = 0.132\times\left(\frac{2.0}{0.32}\right) = 0.825\,\text{mA/V}^2$$

$$K_N = k'_N\frac{W_n}{L_n} = 0.334\times\left(\frac{0.9}{0.32}\right) = 0.939\,\text{mA/V}^2$$

These results lead to an average value $K$ = 0.882 mA/V$^2$. The propagation delay follows as

$$t_p = \frac{70\times10^{-12}}{0.882\times10^{-3}}\left[\frac{2\times0.5}{(2.5-0.5)^2}+\frac{2}{(2.5-0.5)}\ln\left(\frac{2.5-0.5}{2.5/2}\right)\right] = \boxed{57.1\,\text{ns}}$$

**Problem 5.2:** From one stage to the next, both gate widths have been scaled up by a factor of four. For the first stage, the device transconductance parameters are unchanged from the values of $K_p$ and $K_N$ obtained for the single-stage configuration,

$$K_{p,1} = 0.825\,\text{mA/V}^2, K_{N,1} = 0.939\,\text{mA/V}^2$$

The load capacitance for the first stage is equal to the input capacitance of the second stage,

$$C_{L,1} = \frac{\varepsilon_{ox}W_{P2}L_{P2}}{t_{ox}}+\frac{\varepsilon_{ox}W_{N2}L_{N2}}{t_{ox}}$$

$$\therefore C_{L,1} = \frac{\left[3.9\times\left(8.85\times10^{-12}\right)\right]\times\left(8.0\times10^{-6}\right)\times\left(0.32\times10^{-6}\right)}{6.0\times10^{-9}} + \frac{\left[3.9\times\left(8.85\times10^{-12}\right)\right]\times\left(3.6\times10^{-6}\right)\times\left(0.32\times10^{-6}\right)}{6.0\times10^{-9}} = 21.4\,\text{fF}$$

The propagation delay is given by

$$t_{p,1} = \frac{21.4\times10^{-15}}{0.882\times10^{-3}}\left[\frac{2\times0.5}{\left(2.5-0.5\right)^2} + \frac{2}{\left(2.5-0.5\right)}\ln\left(\frac{2.5-0.5}{2.5/2}\right)\right] = 17.5\,\text{ps}$$

For the second stage,

$$K_{p,2} = k_p'\frac{W_{p2}}{L_{p2}} = 0.132\times\left(\frac{8.0}{0.32}\right) = 3.3\,\text{mA/V}^2$$

$$K_{N,2} = k_N'\frac{W_{N2}}{L_{N2}} = 0.334\times\left(\frac{3.6}{0.32}\right) = 3.76\,\text{mA/V}^2$$

which gives an average of 3.53 mA/V$^2$. Since the load capacitance for the second stage is equal to the input capacitance for the third stage, we write

$$C_{L,2} = \frac{\varepsilon_{ox}W_{P3}L_{P3}}{t_{ox}} + \frac{\varepsilon_{ox}W_{N3}L_{N3}}{t_{ox}}$$

$$\therefore C_{L,2} = \frac{\left[3.9\times\left(8.85\times10^{-12}\right)\right]\times\left(32\times10^{-6}\right)\times\left(0.32\times10^{-6}\right)}{6.0\times10^{-9}} + \frac{\left[3.9\times\left(8.85\times10^{-12}\right)\right]\times\left(14.4\times10^{-6}\right)\times\left(0.32\times10^{-6}\right)}{6.0\times10^{-9}} = 85.4\,\text{fF}$$

The propagation delay follows as

$$t_{p,2} = \frac{85.4\times10^{-15}}{3.53\times10^{-3}}\left[\frac{2\times0.5}{\left(2.5-0.5\right)^2} + \frac{2}{\left(2.5-0.5\right)}\ln\left(\frac{2.5-0.5}{2.5/2}\right)\right] = 17.4\,\text{ps}$$

Now, for the third stage,

$$K_{p,3} = k_p'\frac{W_{p3}}{L_{p3}} = 0.132\times\left(\frac{32}{0.32}\right) = 13.2\,\text{mA/V}^2$$

$$K_{N,3} = k_N'\frac{W_{N3}}{L_{N3}} = 0.334\times\left(\frac{14.4}{0.32}\right) = 15.0\,\text{mA/V}^2$$

The average is 14.1 mA/V$^2$. The capacitance load for the third stage is $C_{L,3}$ = 70 pF. The delay time for the third stage is calculated to be

$$t_{p,3} = \frac{70\times10^{-12}}{14.1\times10^{-3}}\left[\frac{2\times0.5}{\left(2.5-0.5\right)^2} + \frac{2}{\left(2.5-0.5\right)}\ln\left(\frac{2.5-0.5}{2.5/2}\right)\right] = 3.57\,\text{ns}$$

The total delay time is

$$t_p = t_{p,1} + t_{p,2} + t_{p,3} = 17.5\,\text{ps} + 17.4\,\text{ps} + 3.57\,\text{ns} = \boxed{3.60\,\text{ns}}$$

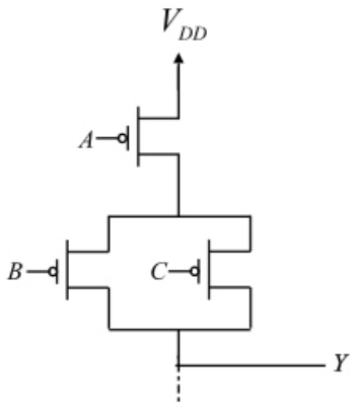
That is to say, the use of two buffer stages with a scaling factor of 4 reduced the propagation delay by a factor close to 1/16 (i.e., down to 3.60 ns from an initial value of 57.1 ns). This is because the buffer stages increased the current-driving capability by 16 without adding appreciable propagation delays of their own.

## P.6 ➡ *Solution*

**Problem 6.1:** The pull-down network consists of a single transistor with *A* supplied to its gate, in one branch, and a pair of transistors in series with gate inputs *B* and *C*, in the other branch. Clearly, the Boolean function implemented is

$$\boxed{Y = A + BC}$$

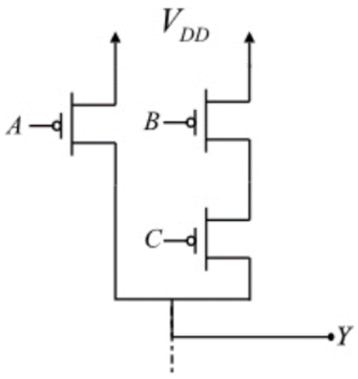
The pull-up network is composed of a transistor controlled by *A* in series with two parallel transistors controlled by *B* and *C*, as shown.




**Problem 6.2:** The pull-down network consists of a single transistor with input *A* connected to its gate and two transistors in parallel fed with inputs *B* and *C*. The Boolean function implemented by the circuit is

$$\boxed{Y = A\left(B + C\right)}$$

The corresponding pull-up network is shown below.



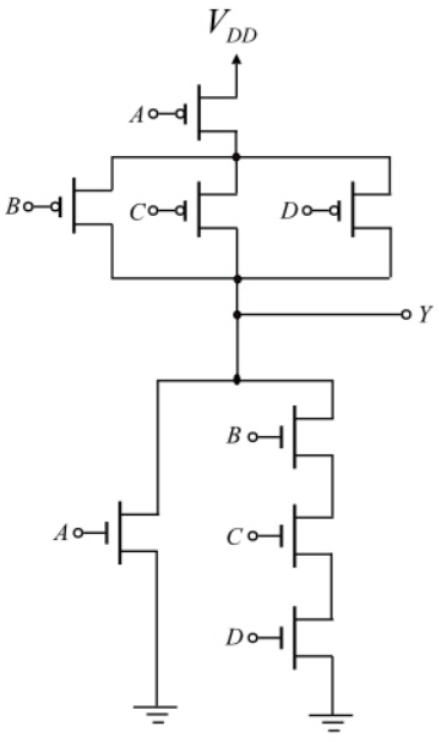

**Problem 6.3:** Inspecting the pull-up network, it is easy to see that

$$\overline{Y} = A + BCD$$

Complementing both sides and manipulating,

$$\overline{Y} = A + BCD \rightarrow \overline{\overline{Y}} = \overline{A + BCD}$$
$$\therefore \overline{\overline{Y}} = Y = \left(\overline{A}\right)\left(\overline{BCD}\right)$$
$$\therefore Y = \overline{A}\left(\overline{B} + \overline{C} + \overline{D}\right)$$
$$\therefore \boxed{Y = \overline{A}\overline{B} + \overline{A}\overline{C} + \overline{A}\overline{D}}$$

The complete logic circuit, including the pull-down network, is shown below.

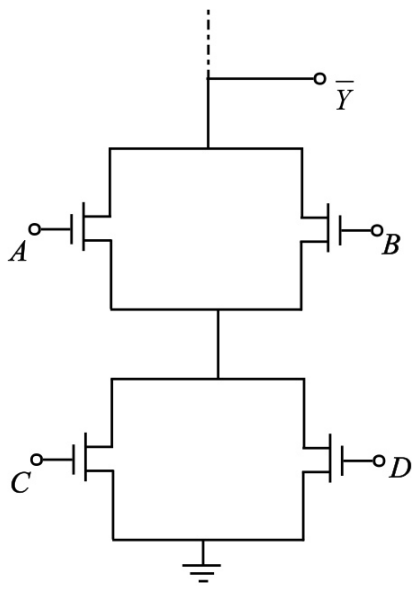


## P.7 ➡ *Solution*

**Problem 7.1:** Let's start with the pull-down network. Complementing both sides of the expression we were given, we get

$$Y = \overline{(A+B)(C+D)} \rightarrow \overline{Y} = \overline{\overline{(A+B)(C+D)}}$$
$$\therefore \overline{Y} = (A+B)(C+D)$$

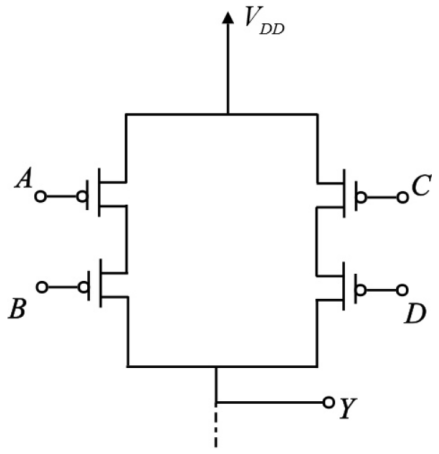
The PDN is drawn below.




Next, before establishing the pull-up network, we simplify the equation for $Y$ a little,

$$Y = \overline{(A+B)(C+D)} \rightarrow Y = \left(\overline{A+B}\right) + \left(\overline{C+D}\right)$$
$$\therefore Y = \overline{A}\,\overline{B} + \overline{C}\,\overline{D}$$

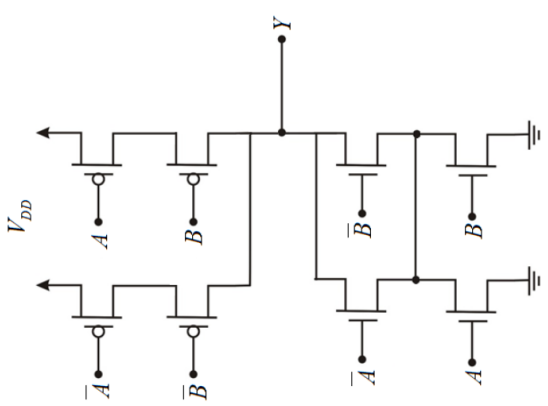
This equation is implemented with the following network,




**Problem 7.2:** Recalling that $\overline{\overline{Y}} = Y$, we take the complement of the logic function twice and manipulate,

$$Y = AB + \overline{A}\,\overline{B} \rightarrow \overline{\overline{Y}} = Y = \overline{\overline{AB + \overline{A}\,\overline{B}}}$$
$$\therefore Y = \overline{\left(\overline{AB}\right)\left(\overline{\overline{A}\,\overline{B}}\right)}$$
$$\therefore Y = \overline{\left(\overline{A}+\overline{B}\right)(A+B)}$$

Equipped with this modified relationship, we sketch the following CMOS network,



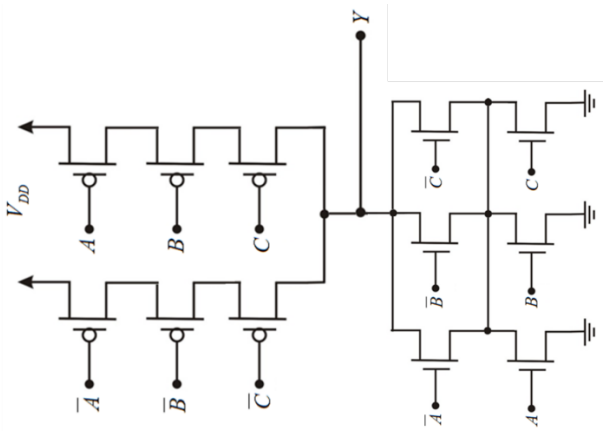
**Problem 7.3:** The equation at hand is similar to the equivalence function studied in the previous problem. Some elementary manipulations bring to

$$Y = ABC + \overline{A}\overline{B}\overline{C} \rightarrow \overline{\overline{Y}} = Y = \overline{\overline{ABC + \overline{A}\overline{B}\overline{C}}}$$

$$\therefore Y = \overline{\left(\overline{ABC}\right)\left(\overline{\overline{A}\overline{B}\overline{C}}\right)}$$

$$\therefore Y = \overline{\left(\overline{A} + \overline{B} + \overline{C}\right)\left(A + B + C\right)}$$

Equipped with this modified relationship, we sketch the following CMOS network,




## P.8 ➡ *Solution*

**Problem 8.1:** The digital circuit in question represents the logic equation

$$Z_1 = \overline{AB + C}$$

The corresponding truth table is shown below.

| $A$ | $B$ | $C$ | $Z_1$ |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

**Problem 8.2:** The logic equation represented by the circuit is

$$Z_2 = \overline{AB + C\overline{D}}$$

The truth table is shown in continuation; the table also includes columns for functions $Z_3$ and $Z_4$.

**Problem 8.3:** The logic equation represented by the circuit is

$$Z_3 = \overline{\left(A + \overline{D}\right)\left(B + C\right)}$$

**Problem 8.4:** The logic equation represented by the circuit is

$$Z_4 = \left(A + \overline{D}\right)\left(B + C\right)$$

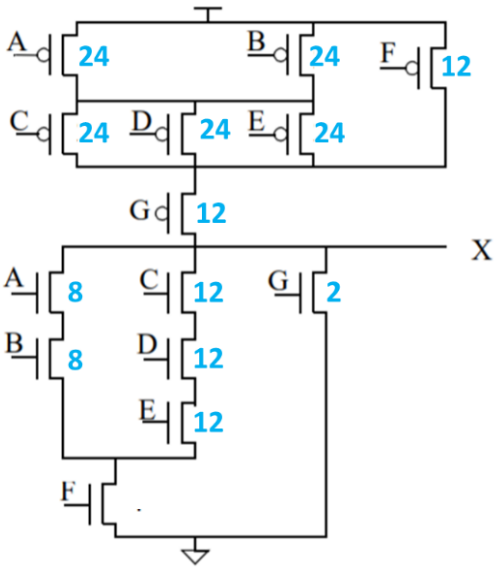
| $A$ | $B$ | $C$ | $D$ | $Z_1$ | $Z_2$ | $Z_3$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 |

## P.9 ➡ *Solution*

We first rewrite the output expression as follows,

$$X = \left(\left(\overline{A} + \overline{B}\right)\left(\overline{C} + \overline{D} + \overline{E}\right) + \overline{F}\right)\overline{G} = \overline{\left(AB + CDE\right)F + G}$$

In this case, we can build the pull-down network by inspection. The pull-up network is the dual of the pulldown network.



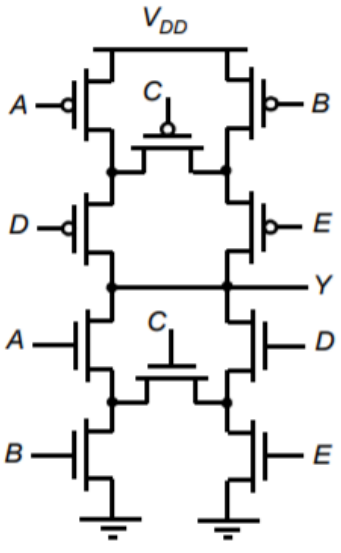

The blue numbers are sizes that meet the requirement – namely, in the worst case the output resistance of the circuit matches the output resistance of an inverter with NMOS width-to-length ratio *W/L* = 2 and PMOS *W/L* = 6.

The worst case pull-up resistance occurs whenever a single path exists from the output node to supply voltage $V_{DD}$. Examples of vector for the worst case are $ABCDEFG$ = 1111100 and 0101110. The best case pull-up resistance occurs when $ABCDEFG$ = 0000000.

The worst case pull-down resistance occurs whenever a single path exists from the output node to ground. Examples of vectors for the worst case are $ABCDEFG$ = 0000001 and 0011110. The best case pull-down resistance occurs when $ABCDEFG$ = 1111111.

## P.10 ➡ *Solution*

The circuit in question is shown below; notice that we have used precisely 10 transistors.

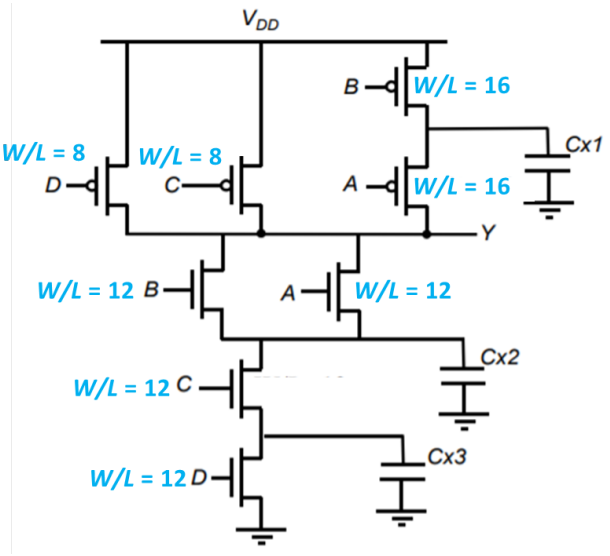



## P.11 ➡ *Solution*

The logic function implemented is

$$Y = \overline{\left(A + B\right)CD}$$

The network is redrawn below with the appropriate transistor sizes shown in blue.




## P.12 ➡ *Solution*

**Problem 12.1:** The two circuits implement the same logic function, namely

$$Y = \left(\overline{ABCD + E}\right) = \left(\overline{A} + \overline{B} + \overline{C} + \overline{D}\right)\overline{E}$$

**Problem 12.2:** No.

**Problem 12.3:** No. Circuit *B* appears optimized for the case where the transistor with input *E* is on the critical path since it is closer to the output node than in circuit *A*. Therefore, if input *E* arrives later, circuit *B* will be faster than circuit *A* since the internal node will already be charged and only the output resistance needs to be switched. Even if we assume all inputs arrive at the same time, however, the two circuits' rise and fall times will not be equal to each other. Consider an input combination where *E*, *A*, *B*, *C*, and *D* are all low. Circuit *A* has only one body-affected device while circuit *B* has four. Since the associated rise in threshold voltage $V_t$ and fall in output resistance affects only one resistor in circuit *A*, but four parallel resistors in circuit *B*, we expect a difference in timing waveforms.

**Problem 12.4:**

→ The lowest output resistance is obtained when all inputs (*A*, *B*, *C*, *D*, and *E*) are equal to 1. In that case, the output resistance is the parallel of the resistance of a NMOS of width 1, with a series of four equal NMOS of width 4. Both combinations have the same resistance, equal to the worst-case output resistance, namely 13 kΩ. It follows that the output resistance in this case is half of this value, or 6.5 kΩ.

→ The lowest output resistance is obtained when all inputs (*A*, *B*, *C*, *D*, and *E*) are equal to 0. Each of the PMOS have the same width, so all of them have the same resistance. The worst case resistance happens when only one of the inputs (*A*, *B*, *C*, or *D*) is equal to 0 while all the rest are equal to 1. The output resistance in that case is the series of the resistance of two of the PMOS and equals 13 kΩ. Then, each of the PMOS has an output resistance equal to 6.5 kΩ. The output resistance is equal to the series of one of these resistances with the parallel of four of the same resistances. Then, the minimum output resistance is 6.5 kΩ + 6.5/4 = 8.125 kΩ.

## P.13 ➡ *Solution*

Both circuits *A* and *B* implement the XOR logic function. Circuit *A* has a dual network because the pull-up network is dual with the pull-down network. However, circuit *B* is still a valid static logic gate, because for any combination of inputs there is either a low resistance path from $V_{DD}$ or ground to the output. Circuit *B* has an extra advantage: The internal node capacitances are less compared to circuit *A*, which makes circuit *B* faster than circuit *A*.

## P.14 ➡ *Solution*

**Problem 14.1:** The truth table is shown below; *A* and *B* are inputs, and *C* is the output.

| *A* | *B* | *C* |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Notice that there one input combination that yields a logic-0 output; accordingly, $N_0 = 1$. Likewise, there are three input combinations that yield a logic-1 output, therefore $N_1 = 3$. Noting that $N = 2$ is the number of input signals feeding the logic circuit, we calculate

$$\alpha_{0\to1} = \frac{N_0\left(2^N - N_0\right)}{2^{2N}} = \frac{1\times\left(2^2-1\right)}{2^{2\times2}} = \boxed{0.188}$$

**Problem 14.2:** Equipped with the pertaining data and the $\alpha_{0\to1}$ coefficient determined just now, we write

$$P = \frac{1}{2}\alpha_{0\to1}C_L V_{DD}^2 f_{clk} = \frac{1}{2}\times0.188\times\left(200\times10^{-15}\right)\times1.5^2\times10^9 = \boxed{42.3\,\mu\text{W}}$$

**Problem 14.3:** Noting that each gate can transition from 1 to 0 or 0 to 1, we take twice the value of $\alpha_{0\to1}$, that is, 2 × 0.188 = 0.376. Since 20% of the gates are switching, we ultimately have

$$\Pi = 0.20\times P\times\left(\text{No. Gates}\right) = 0.20\times42.3\times10^6 = \boxed{8.46\,\text{W}}$$

The power dissipated increases rapidly with increasing number of gates, and is somewhat moderated by lower activity coefficients.

## P.15 ➡ *Solution*

**Problem 15.1:** The truth table is drawn below.

| A | B | C | D | E | F |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 |

The transition probability $\alpha_{0\to1}$ is made up of three contributions: one from wire *D*, a second one from wire *E*, and a third from wire *F*; mathematically,

$$\alpha_{0\to1} = \left(\alpha_{0\to1}\right)_D + \left(\alpha_{0\to1}\right)_E + \left(\alpha_{0\to1}\right)_F \quad \text{(I)}$$

To compute $(\alpha_{0\to1})_D$, we refer to the column representing *D* in the truth table and verify that 2 of the 8 logic combinations culminate with *D* in a logic-0 state, while the other 6 involve *D* in a logic-1 state. Accordingly, we write

$$\left(\alpha_{0\to1}\right)_D = \left(p_0 p_1\right)_D = \frac{2}{8}\times\frac{6}{8} = 0.188$$

Proceeding similarly for $(\alpha_{0\to1})_E$ and $(\alpha_{0\to1})_F$, we get

$$\left(\alpha_{0\to1}\right)_E = \left(p_0 p_1\right)_E = \frac{4}{8}\times\frac{4}{8} = 0.250$$

$$\left(\alpha_{0\to1}\right)_F = \left(p_0 p_1\right)_F = \frac{7}{8}\times\frac{1}{8} = 0.109$$

Substituting in (I),

$$\alpha_{0\to1} = 0.188 + 0.250 + 0.109 = \boxed{0.547}$$

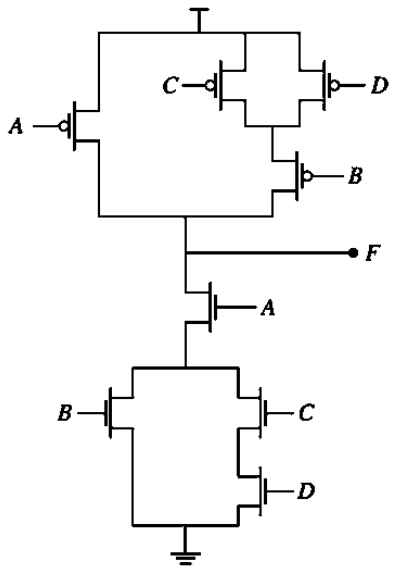
**Problem 15.2:** To establish the power dissipation in a 0 → 1 transition, we substitute the newly obtained $\alpha_{0\to1}$ and other pertaining data into the relation

$$P = \frac{1}{2}\alpha_{0\to1}C_L V_{DD}^2 f_{clk} = 0.5\times0.547\times\left(50\times10^{-15}\right)\times2.0^2\times\left(1.5\times10^9\right)$$

$$\therefore \boxed{P = 82.1\,\mu\text{W}}$$

## P.16 ➡ *Solution*

**Problem 16.1:** The transistor network is shown below.




**Problem 16.2:** Drawing up the truth table is a straightforward task. Note that there are 16 logic combinations.

| *Inputs* | | | | $F = A(B + CD)$ |
|---|---|---|---|---|
| *A* | *B* | *C* | *D* | |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Eleven of the 16 logic combinations culminate with *F* equal to a logic-0, whereas 5 combinations lead to a logic-1 result; it follows that

$$\alpha_{0\to1} = p_0 p_1 = \frac{11}{16}\times\frac{5}{16} = 0.215$$

and, similarly,

$$\alpha_{1\to0} = p_1 p_0 = \frac{5}{16}\times\frac{11}{16} = 0.215$$

so that

$$\alpha_{\text{Total}} = \alpha_{0\to1} + \alpha_{1\to0} = 0.215 + 0.215 = \boxed{0.430}$$

**Problem 16.3:** To find the expected power dissipation, we substitute the pertaining data in

$$P = \frac{1}{2}\alpha_{0\to1} C_L V_{DD}^2 f_{clk} = 0.5\times0.430\times\left(115\times10^{-15}\right)\times1.2^2\times\left(1.6\times10^9\right)$$

$$\therefore \boxed{P = 57.0\,\mu\text{W}}$$

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