

PE Electrical: Electronics and Communications 35 Practice Problems

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Here's a set of 35 simple solved problems for applicants to the PE Electrical: Electronics, Controls, and Communications exam. All problems are fully solved, as usual. This particular problem set covers electronics and communications; we'll tackle control systems engineering in a separate problem set.

Problem Range	Subject	Weight
1 - 13	Basic Electronics	37%
14 - 20	Digital Systems	20%
21 - 27	Electromagnetics	20%
28 – 35	Communications	23%

PROBLEMS

Problem 1. A germanium diode is operated at a junction temperature of 25°C. For a forward current of 10 mA, the forward voltage drop v_D is found to be 0.32 V. Use 25 mV as the thermal voltage. If v_D is increased to 0.4 V, the forward current (mA) becomes, most nearly:

- (A) 104
- **(B)** 154
- **(C)** 204

(D) 254

Problem 2. The reverse saturation current (nA) of the germanium diode introduced in the previous problem is, most nearly:

- (A) 2.76 (B) 27.6
- **(C)** 5.52
- **(D)** 55.2

Problem 3. A MOSFET can be used as a:

(A) Current-controlled capacitor.

(B) Voltage-controlled capacitor.

(C) Current-controlled inductor.

(D) Voltage-controlled inductor.

Problem 4. In a MOSFET operating in the saturation region, the channel length modulation effect causes:

(A) A decrease in the device's output resistance.

(B) A decrease in the unity-gain cutoff frequency.

(C) A decrease in transconductance.

(D) An increase in the gate-source capacitance.

Problem 5. According to the Deal-Grove model of silicon oxidation, the reaction rate is:

(A) Always linear with respect to time.

(B) Linear for small values of time and parabolic for large values of time.

(C) Parabolic for small values of time and linear for large values of time.

(D) Always parabolic with respect to time.

Problem 6. In the context of a common-emitter amplifier, the so-called Miller effect explains:

(A) An increase in the low-frequency cutoff frequency.

(B) An increase in the high-frequency cutoff frequency.

(C) A decrease in the low-frequency cutoff frequency.

(D) A decrease in the high-frequency cutoff frequency.

Problem 7. The drain of an *n*-channel MOSFET is shorted to the gate so that the gate-source voltage equals the drain-source voltage, i.e., $V_{GS} = V_{DS}$. The threshold voltage of the MOSFET is 1.3 V. If the drain current (I_D) equals 2 mA when $V_{GS} = 3$ V, then I_D (mA) for $V_{GS} = 4$ V is, most nearly:

(A) 3

(B) 4

(C) 5

(D) 6

Problem 8. A BJT has a rated power of 18 W and withstands a maximum junction temperature of 182°C. The ambient temperature is 22°C, and the thermal resistance parameters are sink-to-ambient resistance equal to 3.2°C/W and case-to-sink resistance equal to 1.2°C/W. The power (W) that can be safely dissipated in the transistor is, most nearly:

(A) 9

(B) 12

(C) 15

(D) 17.5

Problem 9. The BJT shown in the circuit below has a base-emitter voltage of 0.7 V and a common emitter current gain of 99. The base current (mA) is, most nearly:



(A) 0.03
(B) 3
(C) 0.06
(D) 6

Problem 10. If the input to the ideal comparator shown in the figure is a sinusoidal signal of 8 V (peak-to-peak) without any DC components, then the output of the comparator has a duty cycle of:



(A) 1/2
(B) 1/3
(C) 1/6
(D) 1/12

Problem 11. In the given circuit, if the voltage inputs V_- and V_+ are to be amplified by the same amplification factor, the value of resistance R (k Ω) must be, most nearly:



- (A) 16(B) 33
- **(C)** 41
- **(D)** 66

Problem 12. The following circuit consists of three operational amplifiers. Voltage V_1 at the leftmost node equals 0.1 V. Accordingly, the <u>absolute value</u> of the output voltage V_o (volts) is, most nearly:



Problem 13. In the op-amp circuit illustrated below, assume that the diode current follows the usual voltage-current equation $I = I_s exp(V/V_7)$. It is known that, when input voltage V_i equals 2 V, the output voltage V_0 equals some value V_{01} ; likewise, when input voltage V_i equals 4 V, the output voltage V_0 attains a value V_{02} . What is the relationship between V_{01} and V_{02} ?



(A) $V_{02} = \sqrt{2}V_{01}$ (B) $V_{02} = e^2 V_{01}$ (C) $V_{02} = V_{01} \ln 2$ (D) $V_{01} - V_{02} = V_T \ln 2$

Problem 14. Which of the following Boolean expressions correctly represents the output of the logic circuit illustrated below?



(A) $Y = \bar{A} B + \bar{A} \bar{B} + C$ (B) $Y = \bar{A} B + \bar{A} B + C$ (C) $Y = \bar{A} \bar{B} + A B + C$ (D) $Y = \bar{A} \bar{B} + A B + \bar{C}$

Problem 15. A combinational circuit is illustrated below. Which of the following truth tables correctly describes this logic circuit?



Problem 16. The following flip-flop is constructed using two NAND gates. The unstable state for this device corresponds to which of the following input combinations?

(A) X = 0, Y = 0(B) X = 0, Y = 1(C) X = 1, Y = 0(D) X = 1, Y = 1



Problem 17. In which of the following kinds of register is the data entered one bit at a time and unloaded all at once?

(A) Serial-in, serial-out register

(B) Serial-in, parallel-out register

(C) Parallel-in, serial-out register

(D) Parallel-in, parallel-out register

Problem 18. The sequential network circuit in the diagram below starts with all bits equal to 0. The flip-flops are leading-edge triggered (with a state transition initiated by a change from 0 to 1 on the clock). The clock period is long compared to the flip-flop transition time. Bit 0 is the least significant bit, while bit 2 is the most significant bit. After three clock pulses, what is the count on the circuit (in the sequence bit 0, bit 1, bit 2)?



Problem 19. The activity coefficient $\alpha_{0 \rightarrow 1}$ associated with a transition from 0 to 1 for the 2NAND gate illustrated below is equal to, most nearly:



(A) 0.15
(B) 0.19
(C) 0.24
(D) 0.29

Problem 20. If the 2NAND gate introduced in the previous problem is clocked at 1.5 GHz, fed by a power supply of 1.8 V, and associated with a load of 120 fF (femtofarad), the expected power dissipation (μ W) of the gate for the 0 \rightarrow 1 transition is, most nearly:

(A) 28(B) 42(C) 55

(D) 68

Problem 21. Concentric spherical shells of radii 1 m, 3 m, and 6 m carry uniform surface charge densities equal to 50 nC/m², -40 nC/m², and ρ_s , respectively. The value of ρ_s (nC/m²) required so that the electric flux density be equal to zero at a radial distance of 12 m is, most nearly:

(A) −5

(B) 5

(C) 10

(D) 15

Problem 22. An electric field on a plane is described by a potential function of the form

$$V(r) = 400(r^{-1} + r^{-2})$$

where r is the distance from the source. This field is most likely caused by **(A)** A monopole.

(B) A dipole.

(C) Both a monopole and a dipole.

(D) A quadrupole.

Problem 23. In a source-free region in vacuum, the electrostatic potential $\phi(x,y,z)$ is given by

$$\phi(x, y, z) = 2x^2 + y^2 + mz^2$$

What is the value of constant *m*?

(A) 2 (B) 3

(C) –2

(D) –3

Problem 24. If the electric field intensity in a certain region is given by $\mathbf{E} = (x\mathbf{i} + y\mathbf{j} + z\mathbf{k})$ V/m, the potential difference (V) between two points *P*(3,0,0) and *Q*(1,2,3) is:

(A) −5
(B) −2.5
(C) 2.5
(D) 5

Problem 25. Consider the rectangular loop at rest on the *z*-plane, as shown. The loop is immersed in a region of magnetic flux density $\mathbf{B} = 6x\vec{u}_x - 9y\vec{u}_y + 3z\vec{u}_z$ Wb/m². The magnetic force imparted on the rectangular loop is:



(A) 30*ū*_z N
(B) −30*ū*_z N
(C) 36*ū*_z N
(D) −36*ū*_z N

Problem 26. The electric field of a uniform plane electromagnetic wave is given by

$$\mathbf{E} = \left[2\vec{\mathbf{a}}_{\mathbf{x}} + j3\vec{\mathbf{a}}_{\mathbf{y}} \right] \exp \left[j \left(2\pi \times 10^6 t - 0.25z \right) \right]$$

The polarization of this wave is:

- (A) Right-handed circular
- (B) Right-handed elliptical
- (C) Left-handed circular
- (D) Left-handed elliptical

Problem 27. Which of the following is **not** a form of electromagnetic interference?

(A) Catalytic coupling

(B) Radiated emissions coupling

(C) Magnetic coupling

(D) Conductive coupling

Problem 28. A 5 MHz carrier is amplitude-modulated by a 400 Hz modulating signal to a depth of 75%. If the unmodulated carrier power is 6 kW, the power (kW) of the modulated signal is, most nearly:

(A) 6.4
(B) 6.8
(C) 7.3
(D) 7.7

Problem 29. In a receiver the input signal is 200 μ V, while the internal noise at the input is 20 μ V. With amplification, the output signal voltage is 4 V, while the output noise is 0.8 V. The noise figure of the receiver is:

(A) 0.5(B) 2(C) 2.5

(D) 4

Problem 30. An AM modulator has output given by

$$x(t) = A\cos(450\pi t) + B\cos(400\pi t) + B\cos(500\pi t)$$

The carrier power is 800 W and the efficiency is 45%. The values of A and B are, most nearly: (A) A = 40, B = 18.8

(B) A = 40, B = 25.6(C) A = 50, B = 25.6(D) A = 50, B = 33.3

Problem 31. If a certain computer generates 800,000 ASCII characters per second, the minimum bandwidth (Mbits/sec) required to transmit such a signal will be, most nearly:

(A) 0.7
(B) 1.4
(C) 4.2
(D) 5.6

Problem 32. In a pulse-code modulation system, if the codeword length is increased from 6 to 8 bits, the signal-to-quantization noise ratio improves by a factor equal to:

(A) 16
(B) 32
(C) 64
(D) 128

Problem 33. What is the Nyquist sampling interval for the following signal?

$x(t) = \operatorname{sinc}(800t) + \operatorname{sinc}(600t)$

(A) 1/800 sec
(B) π/800 sec
(C) 1/600 sec
(D) π/600 sec

Problem 34. Frequency modulation, or FM, is an analog communication technique that can be considered analogous to which of the following digital communication technologies?

(A) ASK(B) FSK(C) PSK(D) QAM

Problem 35. A silica optical fiber with a core diameter large enough to be modeled by optical ray theory has a core refractive index of 1.51 and cladding refractive index of 1.46. The acceptance angle (degrees) for this fiber when exposed to air is, most nearly:

- **(A)** 10
- **(B)** 15

(C) 20

(D) 25

≽ ANSWER KEY

Problem	Answer	Problem	Answer
1	D	19	В
2	В	20	С
3	В	21	С
4	Α	22	С
5	В	23	D
6	D	24	С
7	С	25	Α
8	В	26	D
9	С	27	Α
10	В	28	В
11	В	29	В
12	С	30	В
13	D	31	D
14	D	32	Α
15	Α	33	Α
16	Α	34	В
17	В	35	С
18	С		

> SOLUTIONS

1 → D

Appealing to the diode voltage-current relationship, we may write, labeling initial conditions with a subscript 1:

$$i_{D,1} = I_0 \left(e^{v_{D,1}/V_T} - 1 \right)$$

In turn, labeling final conditions with a subscript 2 and dividing one equation by the other, we obtain

$$i_{D,2} = I_0 \left(e^{v_{D,2}/V_T} - 1 \right)$$

$$\therefore \frac{i_{D,2}}{i_{D,1}} = \frac{\sqrt{\left(e^{v_{D,2}/V_T} - 1 \right)}}{\sqrt{\left(e^{v_{D,1}/V_T} - 1 \right)}}$$

$$\therefore i_{D,2} = \frac{e^{v_{D,2}/V_T} - 1}{e^{v_{D,1}/V_T} - 1} i_{D,1}$$

$$\therefore i_{D,2} = \frac{e^{0.4/0.025} - 1}{e^{0.32/0.025} - 1} \times 10 = \boxed{254 \text{ mA}}$$

2 🔿 B

All we have to do is solve the diode equation for I_0 :

$$i_{D,1} = I_0 \left(e^{v_{D,1}/V_T} - 1 \right) \to I_0 = \frac{10}{e^{0.32/0.025} - 1}$$
$$\therefore I_0 = \frac{10 \times 10^{-3}}{e^{0.32/0.025} - 1} = 2.76 \times 10^{-8} \text{ A}$$
$$\therefore \boxed{I_0 = 27.6 \text{ nA}}$$

3 🔿 B

A typical MOSFET is akin to a voltage-controlled capacitor.

4 ➡ A

Channel length modulation affects the output resistance.

5 🔿 B

In the Deal-Grove model of silicon oxidation, reaction rate proceeds linearly for small values of time and parabolically for large values of time.

6 🔿 D

Recall that for the high-frequency response of a common-emitter amplifier, we may write

$$f_{H} = \frac{1}{2\pi C_{\rm in}R_{\rm in}}$$

where the internal capacitance C_{in} is such that

$$C_{\rm in} = C_{\pi} + C_{\mu} \left(1 + g_m R_c \right)$$

The Miller-effect factor $(1 + g_m R_c)$ is always greater than unity and therefore increases the internal capacitance C_{in} , leading to a diminished f_H .

7 🔿 C

The drain current is proportional to the squared voltage difference $(V_{GS} - V_T)^2$, that is,

$$I_D \propto \left(V_{GS} - V_T\right)^2$$

Denoting initial and final conditions by subscripts 1 and 2, respectively, we may write

$$\frac{I_1}{I_2} = \frac{\left(V_{GS,1} - V_T\right)^2}{\left(V_{GS,2} - V_T\right)^2}$$
$$\therefore \frac{2}{I_2} = \left(\frac{3 - 1.3}{4 - 1.3}\right)^2$$
$$\therefore \overline{I_2} = 5.05 \,\mathrm{mA}$$

8 🔿 B

The power dissipated in the transistor is given by

$$P_{D} = \frac{T_{J,\text{max}} - T_{\text{amb}}}{\theta_{\text{dev-case}} + \theta_{\text{case-sink}} + \theta_{\text{sink-amb}}}$$

We have the sink-to-ambient resistance $\theta_{sink-amb}$ and the sink-toambient resistance $\theta_{sink-amb}$, but $\theta_{dev-case}$ is missing; this latter variable is determined as

$$\theta_{\text{dev-case}} = \frac{T_{J,\text{max}} - T_{\text{amb}}}{P_{D,\text{rated}}} = \frac{182 - 22}{18} = 8.89^{\circ} \text{ C/W}$$

so that

$$P_D = \frac{182 - 22}{8.89 + 1.2 + 3.2} = \boxed{12.0 \text{ W}}$$

9 🔿 C

We first apply KVL to the base-emitter loop and solve for emitter current i_E :

$$V_{BB} = V_{BE} + i_E R_E \rightarrow i_E = \frac{V_{BB} - V_{BE}}{R_E}$$

$$\therefore i_E = \frac{8 - 0.7}{1220} = 0.00598 \,\mathrm{A}$$

or, equivalently, $i_E = 5.98$ mA. Applying a current balance to the system and using $i_c = \beta i_B$, we find that

$$i_E = i_B + i_C = i_B + \beta i_B$$
$$\therefore i_E = (1 + \beta) i_B$$
$$\therefore i_B = \frac{i_E}{1 + \beta} = \frac{5.98}{1 + 99} = \boxed{0.0598 \text{ mA}}$$

10 🏟 B

The input signal can be described as $V_i = 4 \sin \omega t$. With $V_i = 2$ V, we obtain

$$2 = 4\sin\omega t \to \sin\omega t = \frac{2}{4}$$
$$\therefore \sin\omega t = \frac{1}{2}$$

But $arcsin(1/2) = \pi/6$, $5\pi/6$ (see the waveform below). Thus, the duty cycle is such that



11 🔿 B

The gain at the inverting terminal is $A^- = -R_f/R_1 = -22/10 = -2.2$, that is, $|A^-| = 2.2$. Now, applying KVL at the non-inverting terminal,

$$V_a = V_+ \left(\frac{R}{R+15}\right)$$

The gain at the non-inverting terminal is, in turn,

$$1 + \frac{R_f}{R_I} = \frac{V_0}{V_+ \left(\frac{R}{R+15}\right)}$$
$$\therefore \frac{V_0}{V_+} = \left(1 + \frac{R_f}{R_I}\right) \times \left(\frac{R}{R+15}\right)$$
$$\therefore \frac{V_0}{V_+} = \left(1 + \frac{22}{10}\right) \times \left(\frac{R}{R+15}\right)$$
$$\therefore \frac{V_0}{V_+} = 3.2 \left(\frac{R}{R+15}\right)$$

But the absolute gain must equal 2.2; accordingly,

$$3.2\left(\frac{R}{R+15}\right) = 2.2$$
$$\therefore R = 33.1 \text{ k}\Omega$$

12 🔶 C

Firstly, amplifier 1 functions as a noninverter and yields a voltage υ_1 such that

$$v_1 = \left(1 + \frac{R_F}{R_I}\right) V_1 = \left(1 + \frac{400}{20}\right) \times 0.1 = 2.1 \text{ V}$$

Amplifier 2 is a buffer and outputs the same voltage that it receives, namely $v_2 = 0.1$ V. Finally, amplifier 3 is a summing amplifier that receives inputs from amps 1 ($v_1 = 2.1$ V) and 2 ($v_2 = 0.1$ V), so that

$$|V_o| = \left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2\right) = \left(\frac{100}{20} \times 2.1 + \frac{100}{10} \times 0.1\right) = \boxed{11.5 \text{ V}}$$

13 🔿 D

Output voltage V_0 equals the voltage V_D across the diode, but with an inverted sign:

$$V_0 = -V_D = -V_T \ln\left(\frac{I}{I_s}\right)$$

Note that when the voltage across the 2 $k\Omega$ resistor equals 2 V, the corresponding current equals 1 mA. Accordingly,

$$V_{01} = -V_T \ln\left(\frac{1.0 \times 10^{-3}}{I_S}\right)$$
(I)

In turn, when the voltage across the 2 k Ω resistor is doubled to 4 V, the current will likewise double to 2 mA. Accordingly,

$$V_{02} = -V_T \ln\left(\frac{2.0 \times 10^{-3}}{I_s}\right) \text{ (II)}$$

Subtracting (II) from (I) and simplifying,

$$V_{01} - V_{02} = -V_T \ln\left(\frac{1.0 \times 10^{-3}}{I_S}\right) + V_T \ln\left(\frac{2.0 \times 10^{-3}}{I_S}\right)$$
$$=V_T \ln 2$$
$$\therefore V_{01} - V_{02} = V_T \ln 2$$

14 🔿 D

Let the output of the XOR gate be X_1 . Since the gate in question is a XOR, we have $X_1 = A \bigoplus B$. It follows that the output of the NAND gate is

$$Y = \overline{X_1 \cdot C} = \overline{\left(A \oplus B\right) \cdot C}$$

Applying de Morgan's law (i.e., $\overline{AB} = \overline{A} + \overline{B}$),

$$Y = \overline{\left(A \oplus B\right).C} = \overline{\left(A \oplus B\right)} + \overline{C}$$

Finally,

$$Y = \overline{\left(A \oplus B\right)} + \overline{C} = \overline{AB + \overline{A}\overline{B} + \overline{C}}$$

15 🔿 A

Let z_1 denote the output of the NOT gate and z_2 denote the output of the XNOR gate. We may write

$$z_1 = \overline{A}$$
; $z_2 = A.B = \overline{A \oplus B}$

Referring to the rightmost XOR gate, we may write $Z = z_1 \bigoplus z_2$, so that

$$Z = z_1 \oplus z_2 = \overline{A} \oplus \overline{A \oplus B}$$
$$\therefore Z = \overline{A} \overline{\overline{A \oplus B}} + \overline{\overline{A}} \cdot \overline{A \oplus B}$$

But $\overline{\overline{A \oplus B}} = A \oplus B$ and $\overline{\overline{A \oplus B}} = AB + \overline{A}\overline{B}$, giving

$$Z = \overline{A} \left(A\overline{B} + \overline{A}B \right) + A \left(AB + \overline{A}\overline{B} \right)$$
$$\therefore Z = A\overline{A}B + \overline{A}\overline{A}B + A.AB + A.\overline{A}\overline{B}$$
$$\therefore Z = 0 + \overline{A}B + AB + 0$$

In the last passage, we've used $A\overline{A} = 0$. Finally, we have, using $A + \overline{A} =$

1,

$$Z = \overline{A}B + AB = B\left(\underbrace{\overline{A} + A}_{=1}\right)$$
$$\therefore Z = B.1$$
$$\therefore Z = B$$

This expression can be used to draw up the following truth table, which matches option (A).

Α	В	Ζ
0	0	0
0	1	1
1	0	0
1	1	1

16 🔿 A

The device actually behaves like an S-R latch; the corresponding truth table is shown below. As highlighted in red, an input X = 0, Y = 0 is considered invalid.

X	Y	Q_n	Q_{n+1}	State
0	0	0	×	Involid
0	0	1	×	Invaliu
0	1	0	1	S a t
0	1	1	1	Set
1	0	0	0	Deest
0	1	1	1	Reset
1	1	0	0	Hold
1	1	1	1	Ποία

17 🔿 B

The data of a SIPO register is entered one bit at a time (hence the phrase *serial-in*) and output all at once (hence the phrase *parallel-out*).

18 🔿 C

The first clock pulse will cause flip-flop 0 to transition. The next state of flip-flop 0 is

$$Q_0^+ = D_0 = \overline{Q}_0 = 1$$

This results in a transition of flip-flop 1, because its clock input changes from 0 to 1 (see the illustration in the problem statement). The output of flip-flop 2 becomes

$$Q_1^+ = D_1 = \overline{Q}_1 = 1$$

This results in a transition of flip-flop 2, because its clock input changes from 0 to 1. The output of flip-flop 2 becomes

$$Q_2^+ = D_2 = \overline{Q}_2 = 1$$

The second clock pulse will cause flip-flop 0 to transition. The next state of flip-flop 0 is then

$$Q_0^+ = D_0 = \overline{Q}_0 = 0$$

This transition from 1 to 0 does not cause flip-flop 1 to transition, so flip-flop 2 does not transition either. The third clock pulse will cause flip-flop 0 to transition. The next state of flip-flop 0 is

$$Q_0^+ = D_0 = \overline{Q}_0 = 1$$

This results in a transition of flip-flop 1, because its clock input changes from 0 to 1. The output of flip-flop 1 becomes

$$Q_1^+ = D_1 = \overline{Q}_1 = 0$$

This transition from 1 to 0 does not cause flip-flop 2 to transition. Finally, the count after three clock pulses is $Q_0 = 1$, $Q_1 = 0$, and $Q_2 = 1$, or 101.

The first step is to prepare a truth table for the 2NAND gate:

Α	В	С
0	0	1
0	1	1
1	0	1
1	1	0

As shown, there is one input combination that yields a logic-0 output, so $N_0 = 1$. Similarly, there are three input combinations that yield a logic-1 output, hence $N_1 = 3$. Noting that N = 2 is the number of input signals feeding the logic circuit, we have

$$\alpha_{0\to 1} = \frac{N_0 \left(2^N - N_0\right)}{2^{2N}} = \frac{1 \times \left(2^2 - 1\right)}{2^{2 \times 2}} = \boxed{0.188}$$

20 🔿 C

Equipped with the pertaining data and the $\alpha_{0 \rightarrow 1}$ coefficient obtained just now, we write

$$\Pi = \frac{1}{2} \alpha_{0 \to 1} C_L V_{DD}^2 f_{clk} = \frac{1}{2} \times 0.188 \times (122 \times 10^{-15}) \times 1.8^2 \times (1.5 \times 10^9) = 5.48 \times 10^{-5} \text{ W}$$

$$\therefore \Pi = 54.8 \,\mu\text{W}$$

21 🔿 C

The electric flux density at r = 12 m (or any other one external point) will equal zero if the total charge of the largest shell is such that the charge balance of the three shells yields zero. Recalling that surface area of a sphere $= 4\pi R^2$, we have

$$50 \times 10^{-9} \frac{\mathrm{nC}}{\mathrm{m}^2} \times \left(4\pi \times 1.0^2\right) \mathrm{m}^2 - 40 \frac{\mathrm{nC}}{\mathrm{m}^2} \times \left(4\pi \times 3.0^2\right) \mathrm{m}^2$$
$$+ \rho_s \frac{\mathrm{nC}}{\mathrm{m}^2} \times \left(4\pi \times 6.0^2\right) \mathrm{m}^2$$
$$\therefore \boxed{\rho_s = 10 \, \mathrm{nC/m^2}}$$

22 🔿 C

The potential function can be restated as

$$V(r) = 400(r^{-1} + r^{-2}) = \frac{400}{r} + \frac{400}{r^2}$$

Compare this equation with the potential associated with a monopole,

$$\left[V(r)\right]_{\text{monopole}} = \frac{\theta}{4\pi Er}$$

and the potential associated with a dipole,

$$\left[V(r)\right]_{\text{dipole}} = \frac{\theta d \cos \theta}{4\pi E r^2}$$

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Since $[V(r)]_{monopole} \propto r^{-1}$ and $[V(r)]_{dipole} \propto r^{-2}$, we surmise that the potential we were given is the superposition of a monopole and a dipole.

23 🔿 D

For a source-free region, the divergence of some particular electric field *E* must equal zero, i.e., $\nabla \cdot E = 0$. Noting that the electric field is related to the potential ϕ by $E = -\nabla \phi$, we have

$$E = -\begin{bmatrix} \frac{\partial}{\partial x} (2x^2 + y^2 + mz^2)\mathbf{i} + \frac{\partial}{\partial y} (2x^2 + y^2 + mz^2)\mathbf{j} \\ + \frac{\partial}{\partial z} (2x^2 + y^2 + mz^2)\mathbf{k} \end{bmatrix}$$
$$\therefore E = -(4x\mathbf{i} + 2y\mathbf{j} + 2mz\mathbf{k})$$

Finally, the value of *m* is calculated to be

$$\nabla \cdot E = -(4+2+2m) = 0$$
$$\therefore \boxed{m = -3}$$

24 🔿 C

The electric potential difference between two points can be obtained by integrating the electric field intensity over the segment that joins the two points:

$$V = -\int \mathbf{E} \cdot d\mathbf{I}$$

$$\therefore V = -\left[\int_{1}^{3} x \, dx + \int_{2}^{0} y \, dy + \int_{3}^{0} z \, dz\right]$$

$$\therefore V = -\left[\frac{x^{2}}{2}\Big|_{1}^{3} + \frac{y^{2}}{2}\Big|_{2}^{0} + \frac{z^{2}}{2}\Big|_{3}^{0}\right]$$

$$\therefore V = -\left[\left(\frac{3^{2}}{2} - \frac{1^{2}}{2}\right) + \left(\frac{0^{2}}{2} - \frac{2^{2}}{2}\right) + \left(\frac{0^{2}}{2} - \frac{3^{2}}{2}\right)\right]$$

$$\therefore V = -(4 - 2 - 4.5) = \boxed{2.5 \text{ V}}$$

25 🔿 A

We first compute cross products $\vec{u}_x \times B$ and $\vec{u}_y \times B$:

$$\mathbf{u}_{x} \times \mathbf{B} = \mathbf{u}_{x} \times \left[6x\mathbf{u}_{x} - 9y\mathbf{u}_{y} + 3z\mathbf{u}_{z} \right] = 3z\mathbf{u}_{y} - 9y\mathbf{u}_{z}$$
$$\mathbf{u}_{y} \times \mathbf{B} = \mathbf{u}_{y} \times \left[6x\mathbf{u}_{x} - 9y\mathbf{u}_{y} + 3z\mathbf{u}_{z} \right] = 3z\mathbf{u}_{x} - 6x\mathbf{u}_{z}$$

Then, we add magnetic forces imparted on each of the four edges:

$$\mathbf{F} = I \int_{1}^{3} dx \mathbf{u}_{x} \times \mathbf{B} + I \int_{1}^{2} dy \mathbf{u}_{y} \times \mathbf{B} + I \int_{3}^{1} dx \mathbf{u}_{x} \times \mathbf{B} + I \int_{2}^{1} dy \mathbf{u}_{y} \times \mathbf{B}$$

$$\therefore \mathbf{F} = I \int_{1}^{3} dx (-9y \mathbf{u}_{z})_{y=1} + I \int_{1}^{2} dy (-6x \mathbf{u}_{z})_{x=3} + I \int_{3}^{1} dx (-9y \mathbf{u}_{z})_{y=2} + I \int_{2}^{1} dy (-6x \mathbf{u}_{z})_{x=1}$$

$$\therefore \mathbf{F} = I \times \begin{bmatrix} (3-1) \times (-9 \times 1) + (2-1) \times (-6 \times 3) \\ -2 \times (-9 \times 2) - 1 \times (-6 \times 1) \end{bmatrix} \mathbf{u}_{z}$$

$$\therefore \mathbf{F} = 5 \times [-18 - 18 + 36 + 6] \mathbf{u}_{z} = \boxed{30 \mathbf{u}_{z} \mathbf{N}}$$

26 🔿 D

Note that for the given equation, component $|E_x| \neq |E_y|$; thus, the wave is elliptically polarized. Note further that, because **E** plots as a counterclockwise-rotating vector, the wave meets the criterion for a left-handed elliptically polarized wave.

27 🔿 A

Catalytic coupling is a chemical process wherein a inertial catalyst aids in a chemical reaction between two hydrocarbons; it is unrelated to electromagnetic interference.

28 🔿 B

All we have to do is apply the usual equation

$$P_t = P_e \left(1 + \frac{\alpha^2}{2}\right)^{1/2} = 6.0 \times \left(1 + \frac{0.75^2}{2}\right)^{1/2} = \boxed{6.79 \,\mathrm{kW}}$$

29 🔿 B

The noise figure is straightforwardly obtained as

$$NF = \frac{S_i / N_i}{S_o / N_o} = \frac{200/20}{4/0.8} = \boxed{2.0}$$

30 🔿 B

The value of A can be obtained from the carrier power $P_c = 800$ W,

$$P_c = \frac{A^2}{2} \to A = \sqrt{2P_c}$$

$$\therefore A = \sqrt{2 \times 800} = \boxed{40}$$

Next, noting that the modulation efficiency is placed at 45%, we may obtain the sideband power P_{sb} :

$$\eta = \frac{P_{sb}}{P_c + P_{sb}} = 0.45 \rightarrow \frac{P_{sb}}{800 + P_{sb}} = 0.45$$
$$\therefore P_{sb} = 655 \,\mathrm{W}$$

Coefficient *B* easily follows:

$$\frac{1}{2}B^2 + \frac{1}{2}B^2 = 655 \rightarrow B = \sqrt{655}$$
$$\therefore B = 25.6$$

31 🔿 D

Recall that the ASCII has $128 (=2^7)$ characters, so that each character, if represented in binary fashion, would require 7 bits. Accordingly, for a stream of 800,000 ASCII characters per second, the minimum bandwidth is 7 × 800,000 = 5,600,000 bits/sec = 5.6 Mbits/sec. Note that some students may be lured to choose option (A), which is the rate of mega*bytes*, not mega*bits*, required to transmit the signal (since 1 byte = 8 bits).

32 🔿 A

The ratio of SNRs can be stated as

$$\frac{(SNR)_2}{(SNR)_1} = \frac{2^{2N_1}}{2^{2N_2}}$$

where $N_{2,1}$ are codeword lengths. With $N_1 = 6$ and $N_2 = 8$, we obtain

$$\frac{(SNR)_2}{(SNR)_1} = \frac{2^{2\times 2}}{2^{2\times 8}} = \frac{2^{12}}{2^{16}} = \frac{1}{2^4} = \boxed{\frac{1}{16}}$$

Thus, increasing the codeword length from 6 to 8 will reduce the SNR by a factor of 16.

33 🔿 A

Recall that the Nyquist sampling rate equals two times the highest frequency of the input or message signal, that is, $f_s = 2f_m$. Restating the signal we were given, we write

$$x(t) = \operatorname{sinc}(800t) + \operatorname{sinc}(600t) = \frac{\sin(800\pi t)}{800\pi t} + \frac{\sin(600\pi t)}{600\pi t}$$

The frequencies of the wave components are then $f_1 = 800\pi/2\pi = 400$ Hz and $f_2 = 600\pi/2\pi = 300$ Hz. The larger frequency is of course 400 Hz. The sampling frequency follows as

$$f_s = 2f_m = 2f_1 = 2 \times 400 = 800 \,\mathrm{Hz}$$

Finally, the Nyquist sampling interval is found to be t = 1/800 sec.

34 🔿 B

Frequency-shift keying, or FSK, is a digital communication scheme akin to frequency modulation technology. The other acronyms offered as alternatives are amplitude-shift keying (ASK), phase-shift keying (PSK), and quadrature amplitude modulation (QAM).

35 🔿 C

We may first compute the numerical aperture NA,

$$NA \equiv \left(n_1^2 - n_2^2\right)^{1/2} = \left(1.51^2 - 1.46^2\right)^{1/2} = 0.345$$

and then the acceptance angle θ_a :

$$\theta_a \equiv \sin^{-1}(NA) = \sin^{-1}(0.345) = 20.2^{\circ}$$



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